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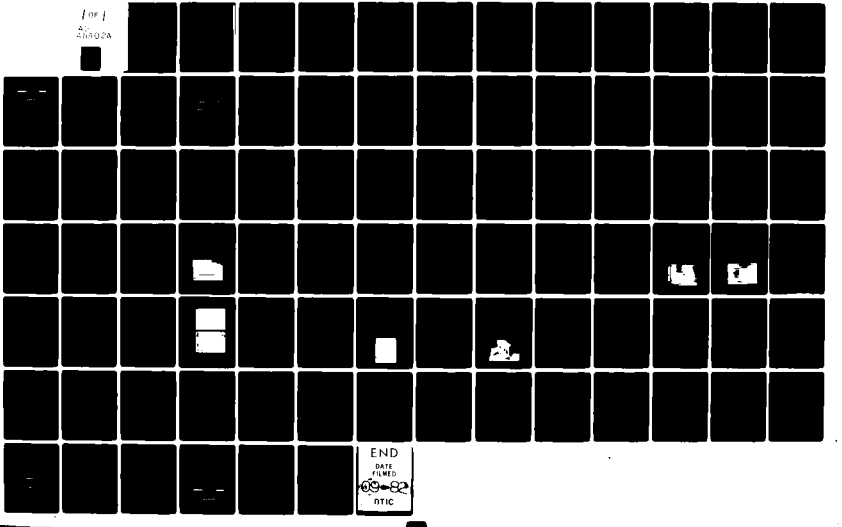

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Near Millimeter Wave Local Oscillator Sources
Proof Of Concepts

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This final report describes research on the demonstration of a new solid state oscillator source principle in a GaAs/AlGaAs heterostructure. The negative differential resistance is based upon a real space transfer of hot electrons from a high mobility GaAs layer to a low mobility AlGaAs layer in the heterostructure. Tunable radiation in the 2-25 MHz range was achieved at a power level of 30 milliwatts in a first device. The potential exists

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to extend this oscillator into the 100-1000 GHz range since the transit time is associated with time of travel between the 100 Å layers in the heterostructure.

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NEAR MILLIMETER WAVE LOCAL OSCILLATOR SOURCES PROOF OF CONCEPTS

1. Introduction - Contract Objective

At the present time, only one solid state electron conduction device (the IMPATT)[1] exists for the generation of electromagnetic radiation in the 100-1000 GHz (3-0.3 mm) range. Laboratory IMPATTS have a power-frequency limit of the order of 1 milliwatt at 230 GHz (Figure 1) that has existed for a number of years and it is doubtful if this limit can be extended much further.

Since 1972, radiation can now be generated at almost every frequency in the spectrum from zero to UV by either and/or conduction current and polarization current devices. Why then has the near millimeter range remained such a challenge? In particular, why can't an efficient solid state source be made in this range?

It was the contract objective to seek new solid state source ideas, do exploratory research and attempt to prove any source concepts that were discovered. Since the last solid state source idea (the Gunn diode)[2] was twenty years ago, this objective posed a real challenge.

2. The Two Basic Methods of Generating Radiation

If one believes in classical radiation theory and Maxwell's equations, then only two basic methods exist for generating radiation. This can be seen from the Maxwell equation

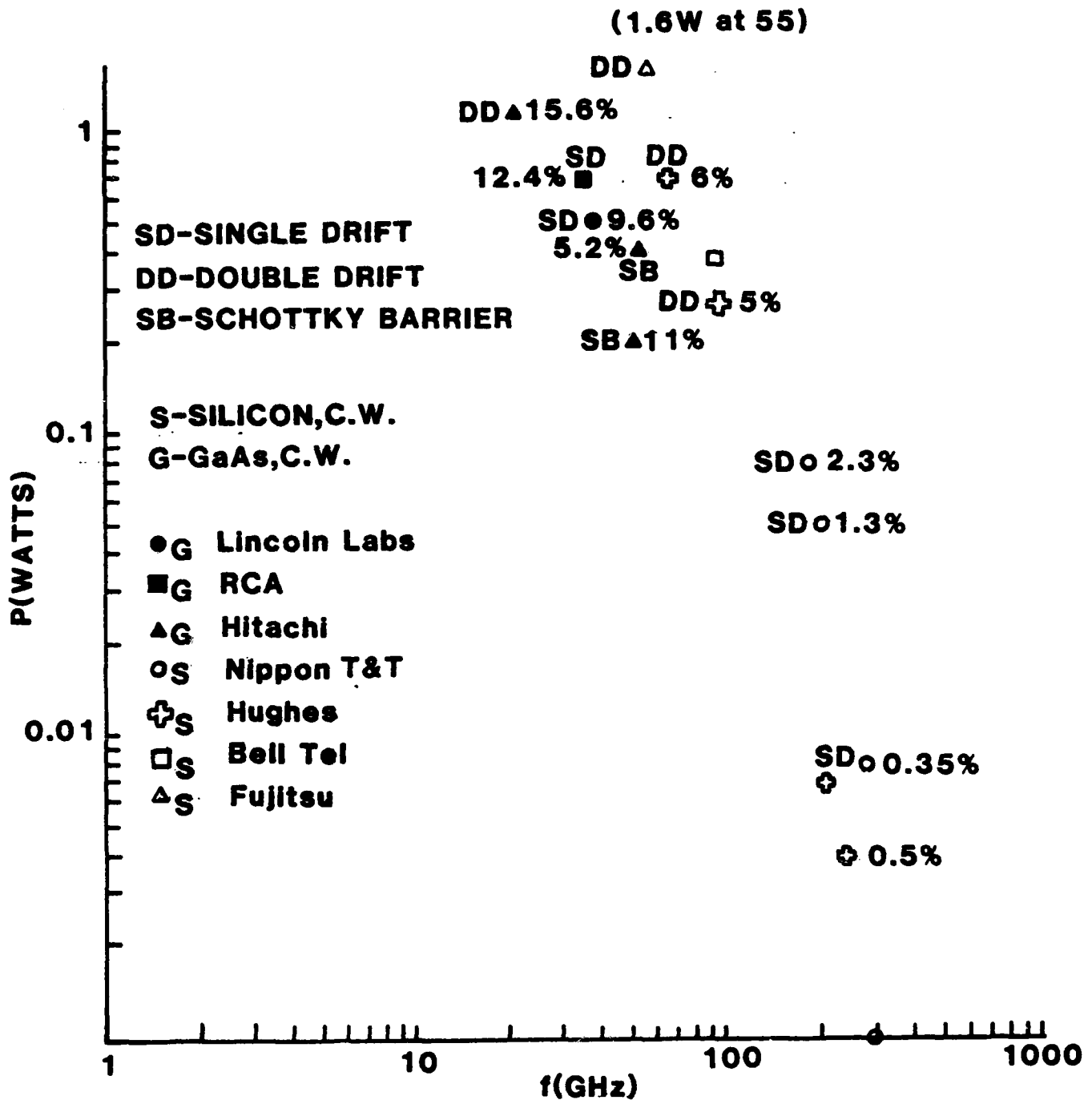

Figure 1. IMPATT Diode State-of-the-Art.

$$\nabla \times H - \varepsilon_0 \frac{\partial \overline{E}}{\partial t} = \overline{J} + \frac{\partial \overline{P}}{\partial t} \qquad (1)$$

where $\overline{J}$ is the conduction and $\frac{\partial \overline{P}}{\partial t}$ the polarization current.

Thus there are conduction current $\overline{J}$ devices and polarization $\frac{\partial \overline{P}}{\partial t}$ (laser) devices.

Examples of conduction current sources are: electron tubes, transistors, Gunns, and IMPATTS. The frequency limitation in a $\overline{J}$ device is transit time.[3] It requires time for electrons to move through the structure which destroys the phase relationship with the electric field.

Hence, if one were to consider a $\overline{J}$ device for the near millimeter region, the device must have a unique feature for minimizing transit time. The structure must be small or have some small dimensions or periodicity in its configuration.

A heterostructure real space electron transfer structure appears ideal for coping with the transit time problem and also for operating in "parallel" to increase the output power.

3. The RSTED Oscillator Principle

In the 15 September 1978 Applied Physics Letters, Hess[4] and colleagues proposed a new mechanism to obtain negative differential resistance in layered heterostructures for conduction parallel to the interface. The mechanism is based on hot electron thermionic emission from high mobility GaAs to low mobility AlGaAs.

This paper came to the attention of P. Coleman during a study contract with Dr. H. Robl of ARO from August 1979-January 1980 on near millimeter wave generation. In a January 1980 report to Dr. Robl, it was recommended that layered GaAs, AlGaAs structures be explored for oscillator possibilities.

Consider the GaAs/AlGaAs heterostructure shown in Figure 2 with a DC bias voltage V_0 and an AC voltage applied parallel to the layered interface.

The current I in the structure is given by the expression

$$I = 2qA_2 n_2 \mu_2 \xi + qA_1 n_1 \mu_1 \xi \qquad (2)$$

where q is the electronic charge, A the area, n the carrier concentration, μ the mobility and ξ the electric field.

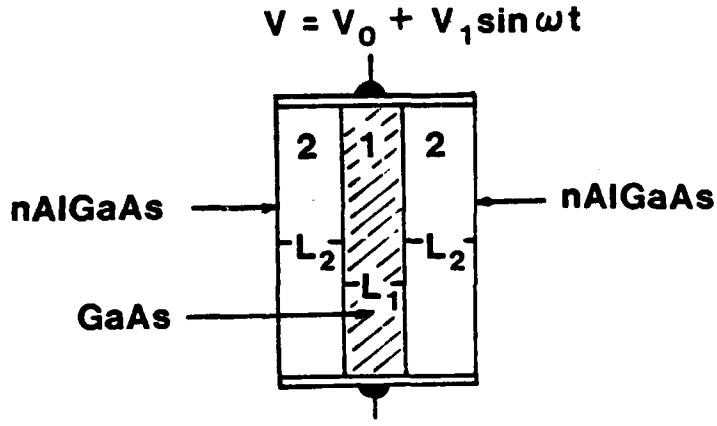

Figure 2. GaAs/AlGaAs heterosturcture.

$$\mu_2(\text{AlGaAs}) << \mu_1(\text{GaAs}) \tag{3}$$

$$\xi = \xi_0 + \xi_1 \sin\omega t \tag{4}$$

The electrons mainly in the GaAs will be periodically heated about some base temperature determined by the DC field ξ_0 and by the AC field $\xi_1 \sin\omega t$. If ξ_0 is sufficiently large to saturate the velocity in the GaAs layer, then

$$I \cong q A_1 n_1 v_s \tag{5}$$

The periodic heating of the electrons in the GaAs will, by thermionic emission, cause a fraction of them to periodically move back and forth between the GaAs and AlGaAs layers. When the AC electric field increases, n_1 and I will decrease thereby achieving a negative differential resistance.

The electron transit time is associated with the transverse dimension of the structure, i.e., the time required to transit the very thin layer thicknesses of the heterostructure.

For example, if one assumes a layer thickness L of 400 Å and a thermal velocity v of 2×10^7 cm/sec, then the transit time t_T would be

$$t_T = \frac{L}{2v} = \frac{2\times10^{-6}}{4\times10^7} = 5\times10^{-12} \text{ sec} . \tag{6}$$

Making layer thickness of 100-500 Å with MBE techniques is no real problem in heterostructure fabrication.

Thus the RSTED oscillator device does require small dimensions to cope with the transit time problem of conduction current devices but this can readily be done in a layered heterostructure. The dimension that must be small is the layer thickness which can be at least an order of magnitude smaller than the critical dimersion in an IMPATT or Gunn device.

The current in a RSTED device depends on the number of pairs of GaAs/AlGaAs layers. For the same field voltage, the current will double if the number of layers are doubled. This is equivalent to operating each pair of levels in parallel to increase the power output. Thus the problem of power combining for a RSTED is non-existent.

4. Proof of RSTED Concept

The two crucial points that must be proven for the suggested RSTED oscillator device are:

1) A negative differential resistance does exist,

2) A NDR is due to real space transfer.

The work of Hess and colleagues[5] during 1979-81 was mainly on measuring the I-ξ curves for various heterojunction samples to see if a negative slope could be observed. Most of their I-ξ curves had nearly flat tops which made the proof of NDR questionable.

A positive proof of NDR is the demonstration of oscillations in a circuit. This was first accomplished in November 1981 with

heterostructure sample #337 using the circuit shown in Figure 3. The resistors R_1 and R_2 provided a voltage divider to apply the DC bias to the oscillator, L and C were the tank circuit components, and C_1 was used to lower the RF resistance in the oscillating circuit.

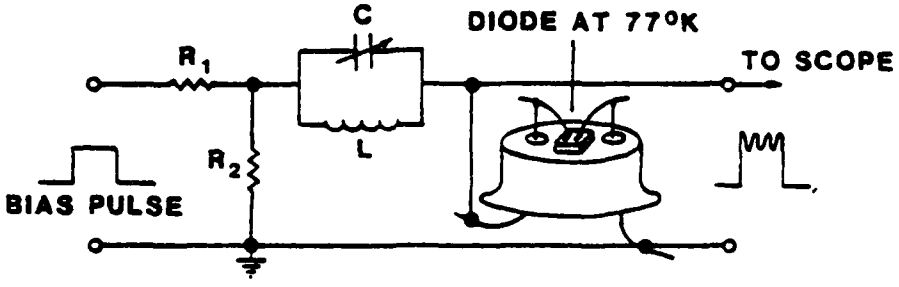

Figure 3. RF oscillator used for RSTED.

The I-ξ curve for sample 337 and the oscillation behavior of the RSTED device are shown in Figure 4. This experiment definitely proved NDR. The circuit broke into oscillation for $V_0 \cong 10$ volts and for $V_0 = 13$ volts, V_1 was measured to be 3 volts with the power output the order of 30 milliwatts at 25 MHz. The frequency could be readily tuned from 2-25 MHz with the L-C components used.

This experiment supports but does not conclusively prove real space transfer. What could be happening is a Gunn effect in

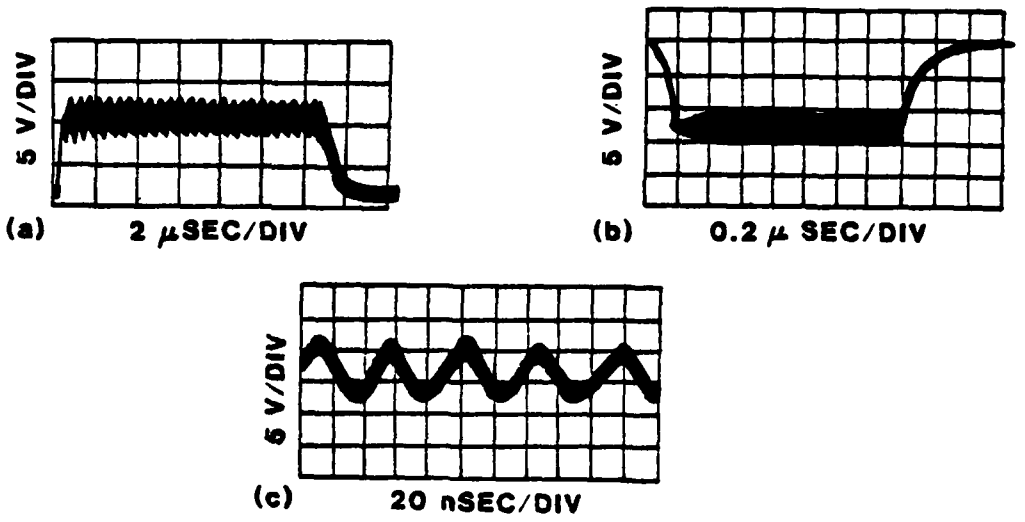

Figure 4. Oscillation behavior of a NDR GaAs/nAlGaAs heterostructure. a) at 2 MHz, b) at 25 MHz, c) at 25 MHz expanded.

either the AlGaAs or GaAs. The fact that the oscillator can be readily tuned over a factor of 10 in frequency rules against a Gunn effect. Also the threshold field for oscillation ($\sim$ 2 kV/cm) is smaller than that for a Gunn oscillator.

A detailed account of these experiments is presented in the two reprints[6,7] included in the Appendix.

5. Heterojunction Properties

While heterojunctions[8] date back over twenty years and have been analyzed by many workers, it is desirable to review some of their properties as they apply to the RSTED oscillator.

Figure 5 gives the band diagrams of an N-n heterojunction. The two cases are the semi-infinite case, i.e., thick layers and the finite case, i.e., thin layers where only depletion and accumulation regions exist, as shown in Figure 6.

In the thick layer case, the current will be carried by both the bulk nAlGaAs and GaAs layers plus the accumulation layer in the GaAs and essentially none by the depletion layer in the nAlGaAs. Hence it would appear that heating the electrons in the accumulation region of the GaAs to move them back into the depletion layer of the nAlGaAs would have a small effect on the total current and result in little if any NDR.

The best case for NDR would appear to be the thin layer case where only depletion-accumulation regions exist. Here moving the electrons from the high mobility accumulation region in the GaAs to the low mobility depletion layer in the nAlGaAs would appreciably change the total current and yield the maximum NDR.

The mathematical problem in calculating the carrier densities $n(x)$ and $p(x)$, the electric field $\xi(x)$ and potential $\phi(x)$, and bending of the band diagrams is solving Poisson's equation in a nice closed form.

The basic equations to be solved are the following:

$$n(x) = N_c e^{(E_F-E_c)/kT} = n_i e^{(E_F-E_i)/kT} = n_i e^{u} \tag{7}$$

$$p(x) = N_v e^{(E_v-E_F)/kT} = n_i e^{-(E_F-E_i)/kT} = n_i e^{-u} \tag{8}$$

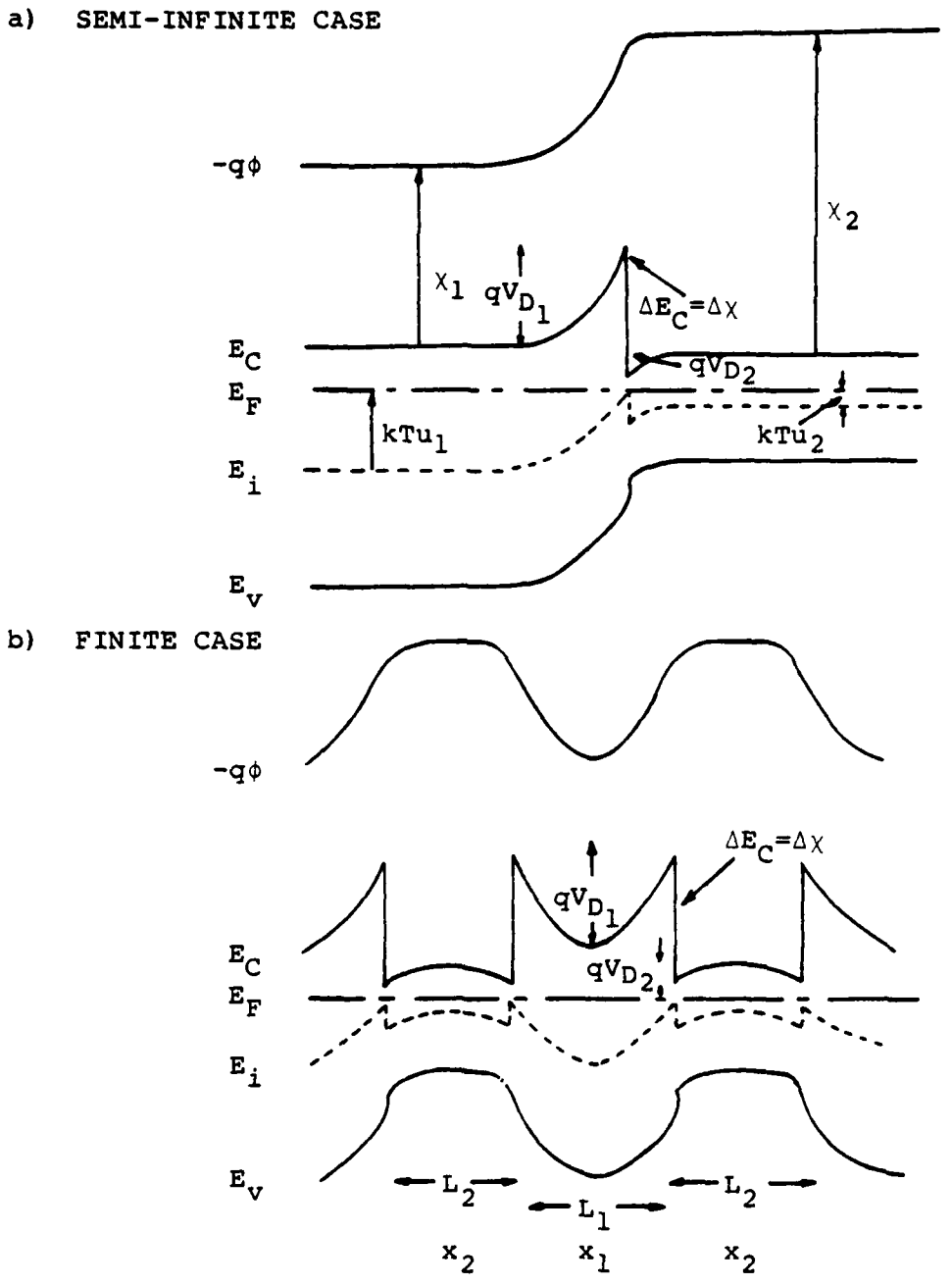

Figure 5. Band diagrams for heterojunction.

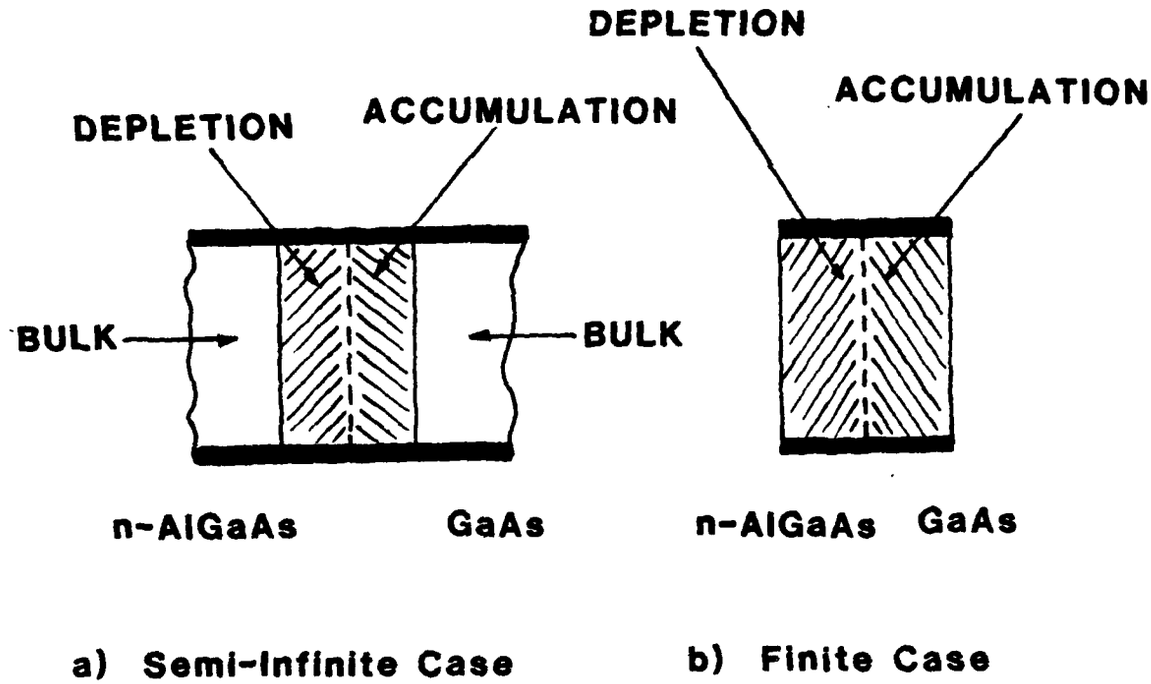

Figure 6. Thick versus thin layer heterojunction.

and

$$\frac{d\xi}{dx}(x) = -\frac{d^2(x)}{dx^2} = \frac{q}{\varepsilon}\left[p-n+N_d^+-N_a^-\right] \tag{9}$$

where the symbols have their standard meanings.

Referring to Figure 5, it can be shown that

$$-q\phi = E_c + \chi = -\left(kTu - E_F - E_g/2 - \chi + \frac{kT}{2}\ln\frac{N_v}{N_c}\right) \tag{10}$$

Let

$$Z = x\sqrt{\frac{2q^2n_i}{\varepsilon kT}}$$

and

$$N_d^+ - N_a^- = 2\,n_i \sinh u_B$$

Then Poisson's equation (9) becomes[9]

$$\frac{d^2u}{dz^2} = \sinh u - \sinh u_B \tag{11}$$

The boundary conditions are:

a) ϕ continuous at interface

b) $-\varepsilon\frac{d\phi}{dx}$ is continuous at interface

c) $\Delta E_C = \chi_2 - \chi_1$ at interface.

For semi-finite case

$$\frac{d\phi}{dx} = 0 \text{ @ } x = \pm\infty$$

For finite case

$$\frac{d\phi}{dx} = 0 \text{ @ the symmetry points } x_1 \text{ and } x_2$$

Multiply Equation (11) by $2\frac{du}{dz}$ and integrate

$$\int_0^{du/dz} d\left(\frac{du}{dz}\right)^2 = 2\int_{u(x_2)}^{u} (\sinh u - \sinh u_B)\, du \tag{12}$$

Then

$$\frac{du}{dz} = \pm\sqrt{2}\left\{[u(x_2) - u]\sinh u_B - [\cosh u(x_2) - \cosh u]\right\}^{\frac{1}{2}} \tag{13}$$

It is at this point that numerical integration is used to complete the problem because of the nonlinear character of the equation. However, T. A. DeTemple[10] has recently suggested that if a change of variables from u back to n is made for the case of electron accumulation that one can obtain an equation for n for which a good closed form approximate solution can be found.

For an n material

$$N_d^+ - N_a^- \approx N_d^+ = 2n_i \sinh u_B \tag{14}$$

Let

$$\beta = \frac{N_d^+}{n(x_2)} \approx \frac{2n_i}{n(x_2)} \sinh u_B < 1 \tag{15}$$

$$\cosh u(x_2) = \frac{e^{u(x_2)} + e^{-u(x_2)}}{2} = \frac{n(x_2)}{2n_i} + \frac{n_i}{2n(x_2)} \approx \frac{n(x_2)}{2n_i} \tag{16}$$

$$\cosh u(x) = \frac{n(x)}{2n_i} + \frac{n_i}{2n(x)} \approx \frac{n(x)}{2n_i} \tag{17}$$

Let

$$F = \frac{n(x)}{n(x_2)} > 1 \tag{18}$$

Substituting in Equation (13) one obtains the equation

$$\frac{1}{F}\frac{dF}{dx} = -2\alpha[F - 1 - \beta \ln F]^{\frac{1}{2}} \tag{19}$$

where

$$\alpha^2 = \frac{q^2 n(x_2)}{2\epsilon kT} \tag{20}$$

Since for the accumulation case $F > 1$ and $\beta < 1$, the $\beta \ln F$ term can be neglected to yield the solution

$$F = \frac{n(x)}{n(x_2)} \cong \sec^2\alpha\,(x_2 - x) = \frac{n_i}{n(x_2)}\, e^u \tag{21}$$

with the electric field

$$\xi(x) = -\frac{kT}{q}\frac{d}{dx}\ln n(x) \cong \frac{2\alpha kT}{q}\tan\alpha\,(x_2 - x) \tag{22}$$

and

$$kTu(x) = [E_F - E_i(x)] = kT \ln\left(\frac{n(x_2)}{n_i}\sec^2\alpha(x_2 - x)\right)$$

or

$$E_i(x) = E_F - kT \ln\left(\frac{n(x_2)}{n_i}\sec^2\alpha\,(x_2 - x)\right) \tag{23}$$

Hence the diffusion potential in the GaAs side of the junction is

$$q V_{D2} = E_i(x_2) - E_i(0) = 2kT \ln(\sec\alpha x_2) \tag{24}$$

If we assume the usual solution for the depletion region in the AlGaAs, then

$$\xi_1(x) \cong \frac{qN_{d1}^+}{\varepsilon_1}(x_1 - x) \tag{25}$$

Matching D fields at the interface yields

$$q N_{d_1}^+ x_1 = \frac{2\varepsilon_2 \alpha kT}{q} \tan \alpha x_2 \tag{26}$$

from which α and $n(x_2)$ can be determined since for the finite case x_1 and x_2 are half the corresponding layer thicknesses. In the depletion case (neglect p-n)

$$\frac{d^2u}{dz^2} \cong -\sinh u_{B_1} \tag{27}$$

Integrating

$$u(x) = [E_F - E_i(x)]/kT = u(x_1) - (x_1 - x)^2 \frac{q^2 n_{i_1}}{\varepsilon_1 kT} \sin u_{B_1} \tag{28}$$

Hence the diffusion potential on the AlGaAs side is seen to be

$$q V_{D_1} = E_i(0) - E_i(x_1) \cong \frac{q^2 n_{i_1} x_1^2}{\varepsilon_1} \sinh u_{B_1} = \frac{q^2 N_{d_1} x_1^2}{2\varepsilon_1} \tag{29}$$

The charge in the accumulation region is

$$q \int_0^{x_2} [N_{d_2}^+ - n(x)]dx = q N_{d_2}^+ x_2 - q \frac{n(x_2)}{\alpha} \tan \alpha x_2 \tag{30}$$

The electron density in the depletion region is

$$n(x) = n_{i_1} e^{u} = n_{i_1} e^{u(x_1)} e^{-a^2(x_1-x)^2} \tag{31}$$

where

$$a^2 = \frac{q^2 n_{i_1}}{\varepsilon_1 kT} \sinh u_{B_1} = \frac{q^2 N_{d_1}^+}{2\varepsilon_1 kT}$$

Hence the charge in the depletion region is

$$q\int_0^{x_1} [N_{d_1}^+ - n(x)]\,dx_1 \cong q N_{d_1}^+ x_1 - q n_{i_1} e^{u(x_1)} \sqrt{\frac{\pi \varepsilon_1 kT}{2q^2 N_{d_1}^+}} \tag{32}$$

Equating charge magnitude from Equations (30) and (32) will yield the value of $u(x_1)$.

A plot of the electron carrier concentration n(x) in the heterostructure has the general shape shown in Figure 7.

6. Thermionic Emission Model

For a thermionic emission model, the "well" configuration of Figure 5b will be assumed with each well having a constant electron concentration n_1 and n_2.

If one uses the thermionic current equation[11]

$$J = q n \sqrt{\frac{kT}{2\pi m^*}}\, e^{-qV/kT} \tag{33}$$

then a current balance yields the relation

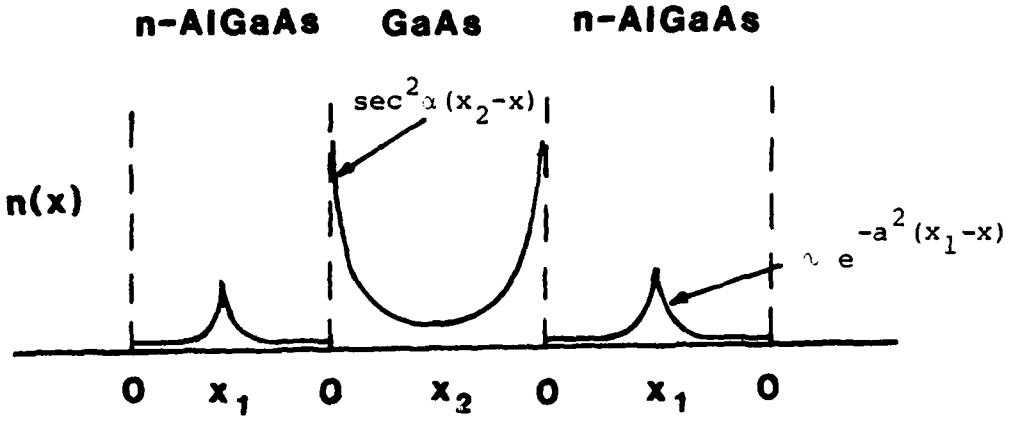

Figure 7. Approximate electron distribution n(x) in the thin heterostructure following Equations (21) and (31).

$$J_{12} = q n_1 \sqrt{\frac{kT_1}{2\pi m_1^*}}\, e^{-qV_1/kT} = J_{21} = q n_2 \sqrt{\frac{kT_2}{2\pi m_2^*}}\, e^{-qV_2/kT} \tag{34}$$

where $qV_1 > qV_2$ are the barrier energies.

Charge conservation requires

$$L_n n_1 + L_2 n_2 = L_1 N_{d_1}^+ \tag{35}$$

The two power balance equations are

$$q L_1 n_1 \mu_1 \xi_0^2 = L_1 n_1 \frac{3k}{2\tau} (T_1 - T_0) + \frac{J_{12}}{q} 3kT_1 - \frac{J_{21}}{q} 3kT_2 \tag{36}$$

and

$$q L_2 n_2 \mu_2 \xi_0^2 = L_2 n_2 \frac{3k}{2\tau} (T_2 - T_0) + \frac{J_{21}}{q} 3kT_2 - \frac{J_{12}}{q} 3kT_1 \tag{37}$$

where τ is the energy relaxation time to the lattice temperature T_0.

It is assumed the mobilities satisfy the inquality

$$\mu_2 << \mu_1 \tag{38}$$

and saturate accurding to the relationship

$$\mu = \mu_0 \left(1 + \frac{q\mu_0 \xi_0^2}{\kappa}\right)^{-\frac{1}{2}} \tag{39}$$

where κ is a constant.

The current equation is given by the formula

$$I = N[L_x L_1 q n_1 \mu_1 \xi_0 + L_x L_2 q n_2 \mu_2 \xi_0] \tag{40}$$

where N is the number of pairs of GaAs/AlGaAs layers.

The problem is now specified with four equations (34), (35), (36) and (37), with four unknowns T_1, T_2, n_1 and n_2, where n_1 is associated with GaAs and n_2 with n AlGaAs.

The equations can be readily solved if the electric field ξ_0 is not too large so that the J_{12} and J_{21} terms in Equations (36) and (37) can be neglected.

Three dimensional I-ξ_0 computer plots are shown in Figures 8-19 for various choices of parameters.

The I-ξ curves of Figure 8, with the mobility μ_{20} variable and qV_1 = 0.394 eV, should be accurate up to ξ the order of 5-6 kV/cm. A low mobility for the nAlGaAs layer is highly desirable.

The curves of Figure 9 indicate that lowering the barrier height qV_1 to 0.19 eV and the mobility μ_{10} to 24,400 cm^2/V-s, causes one to lose much of the NDR of the structure.

The I-ξ curves of Figures 10, 11, and 12 with low barrier heights qV_1 are not significant or accurate except for small field strengths ξ.

The I-ξ curves of Figure 13 with L_1 variable do not show a strong dependence on L_1 although the L_2/L_1 ratio is an important factor.

The I-ξ curves of Figures 14, 15, and 16, with small barrier heights qV_1 are again only accurate for small field strengths ξ.

In comparing I-ξ curves of Figures 13 and 17, the L_2/L_1 ratio effect is more pronounced. A larger L_2/L_1 seems to lead to a large NDR.

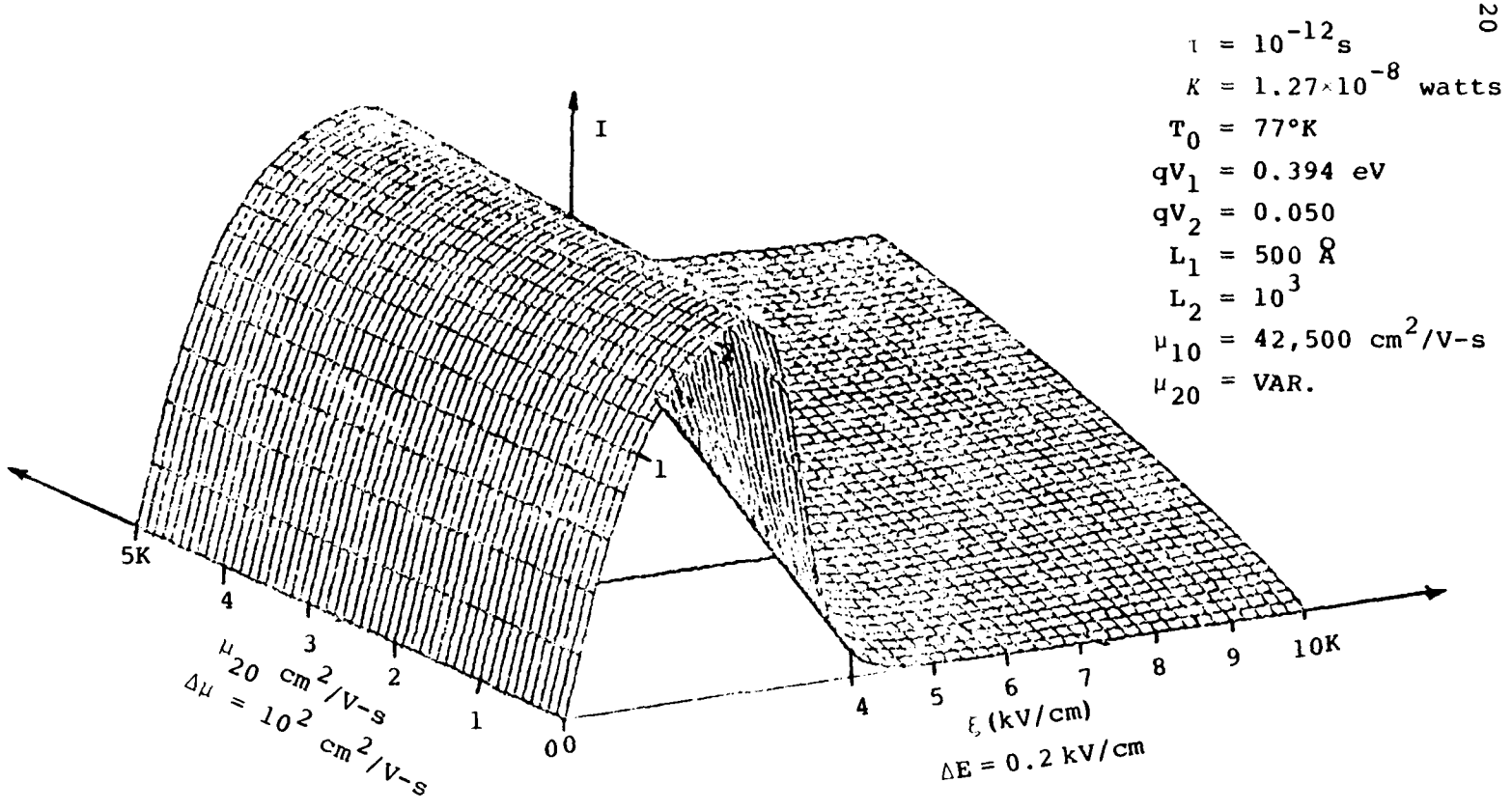

Figure 8. I-ξ curves with AlGaAs mobility μ_{20} variable.

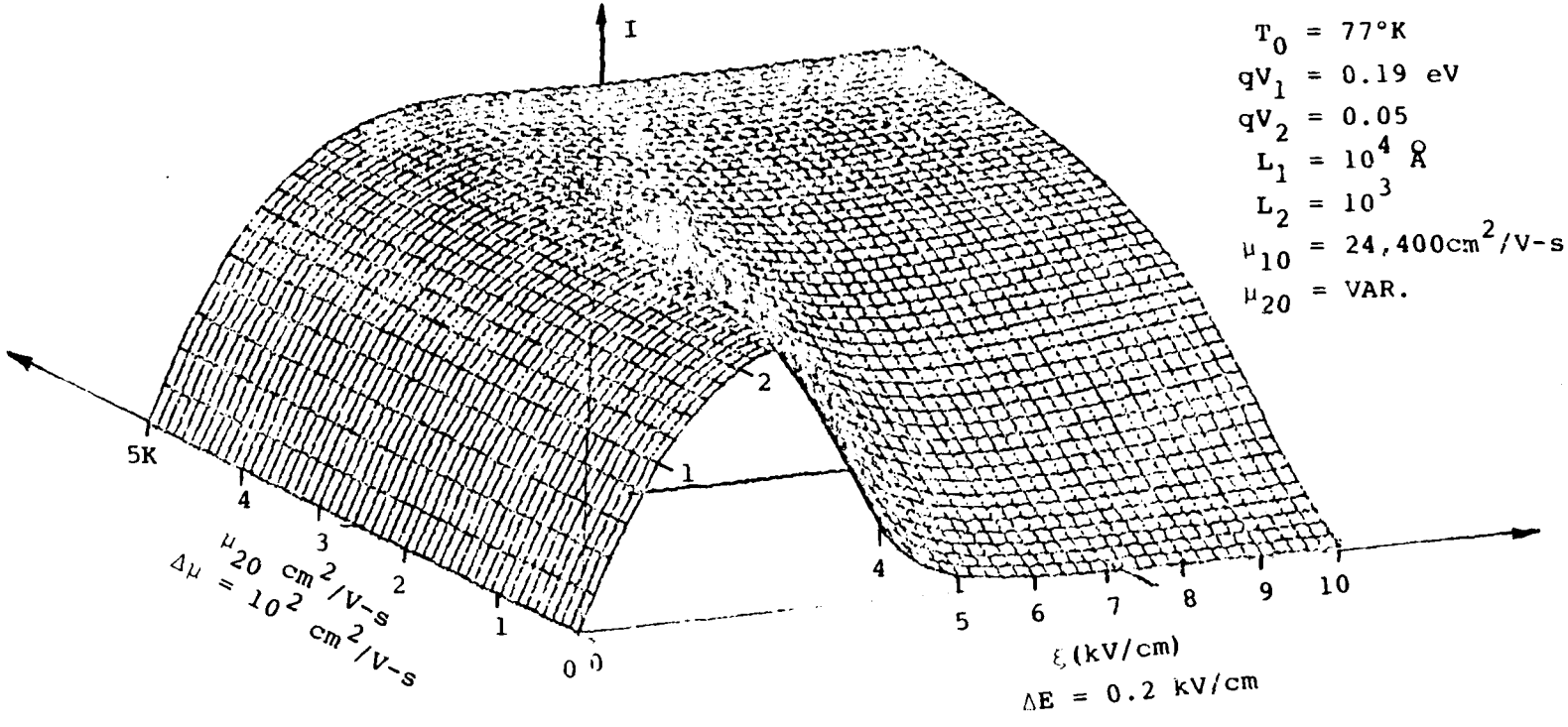

Figure 9. I-ξ curves with AlGaAs mobility μ_{20} variable.

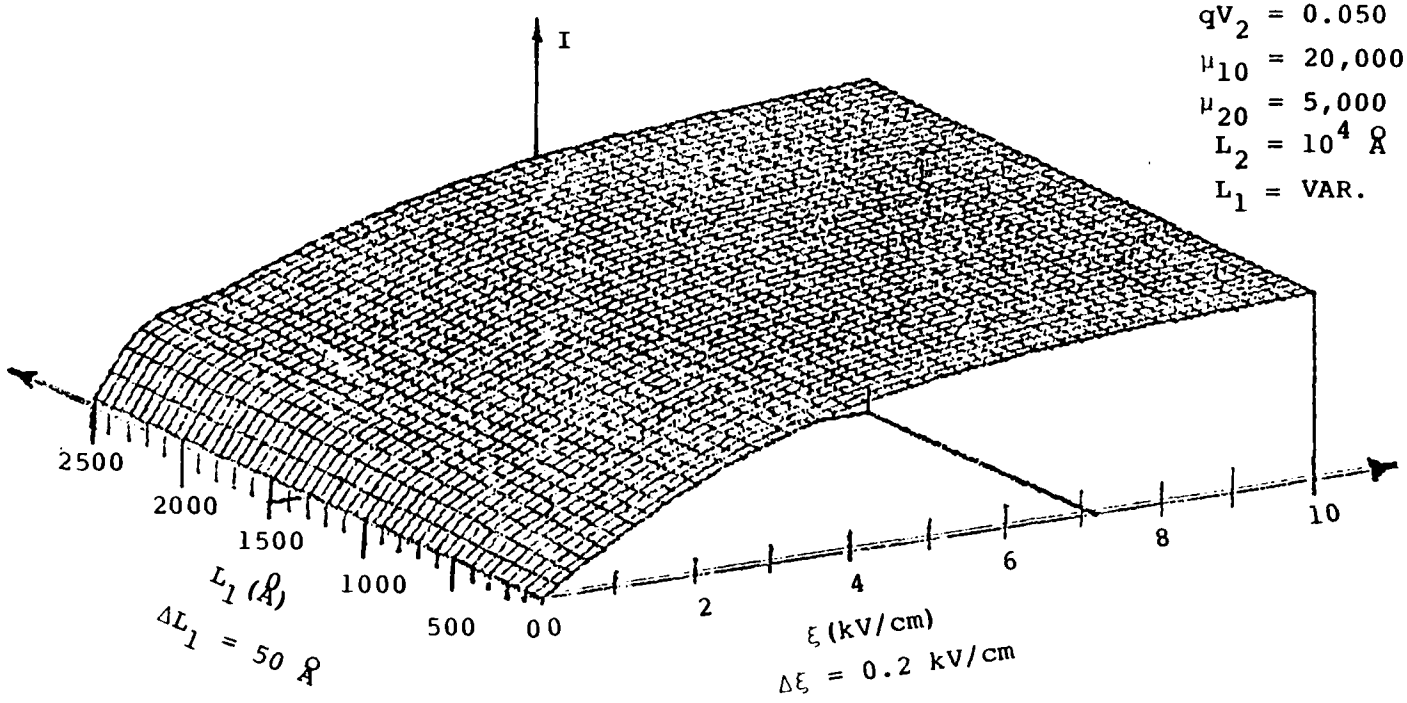

Figure 10. I-ξ curves with GaAs layer thickness L_1 variable.

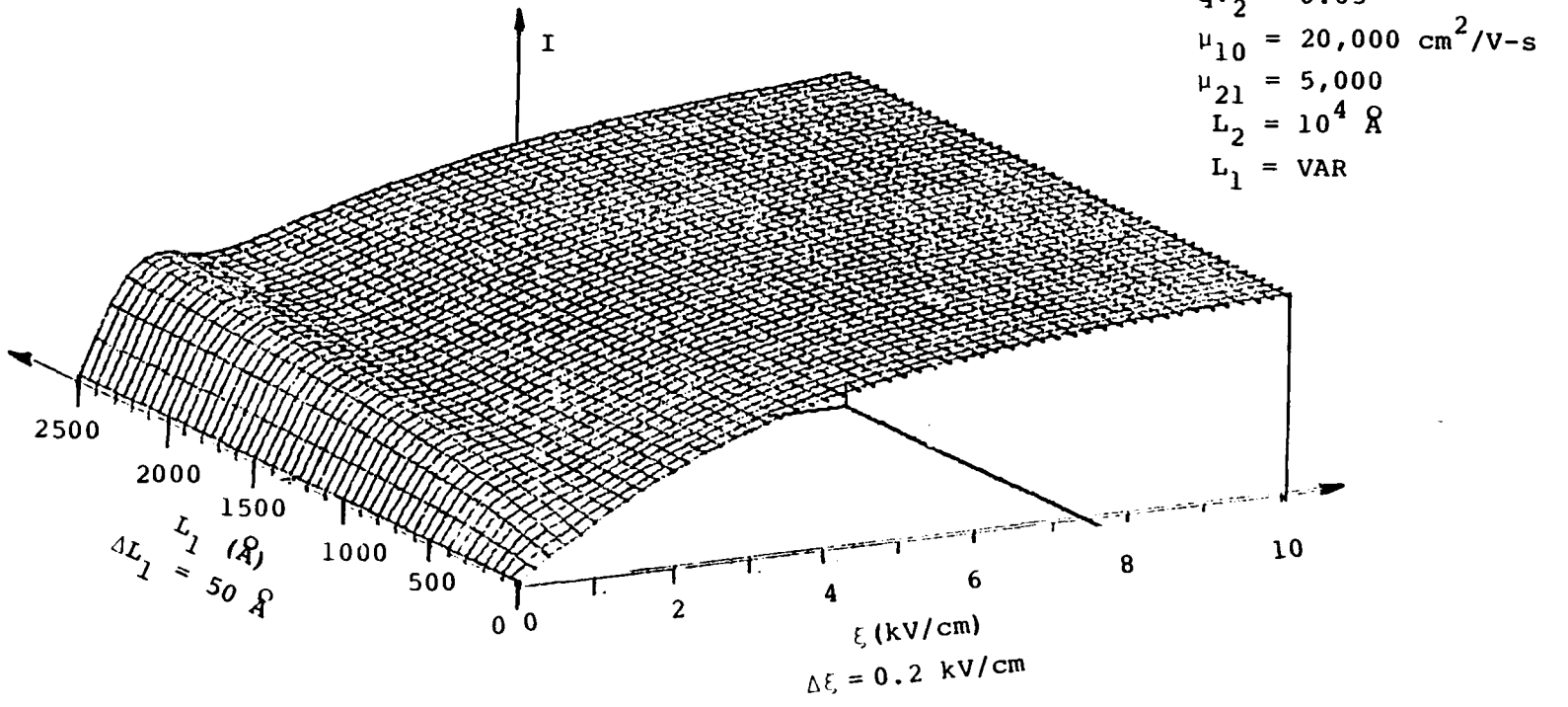

Figure 11. I-ε curves with GaAs layer thickness L_1 variable.

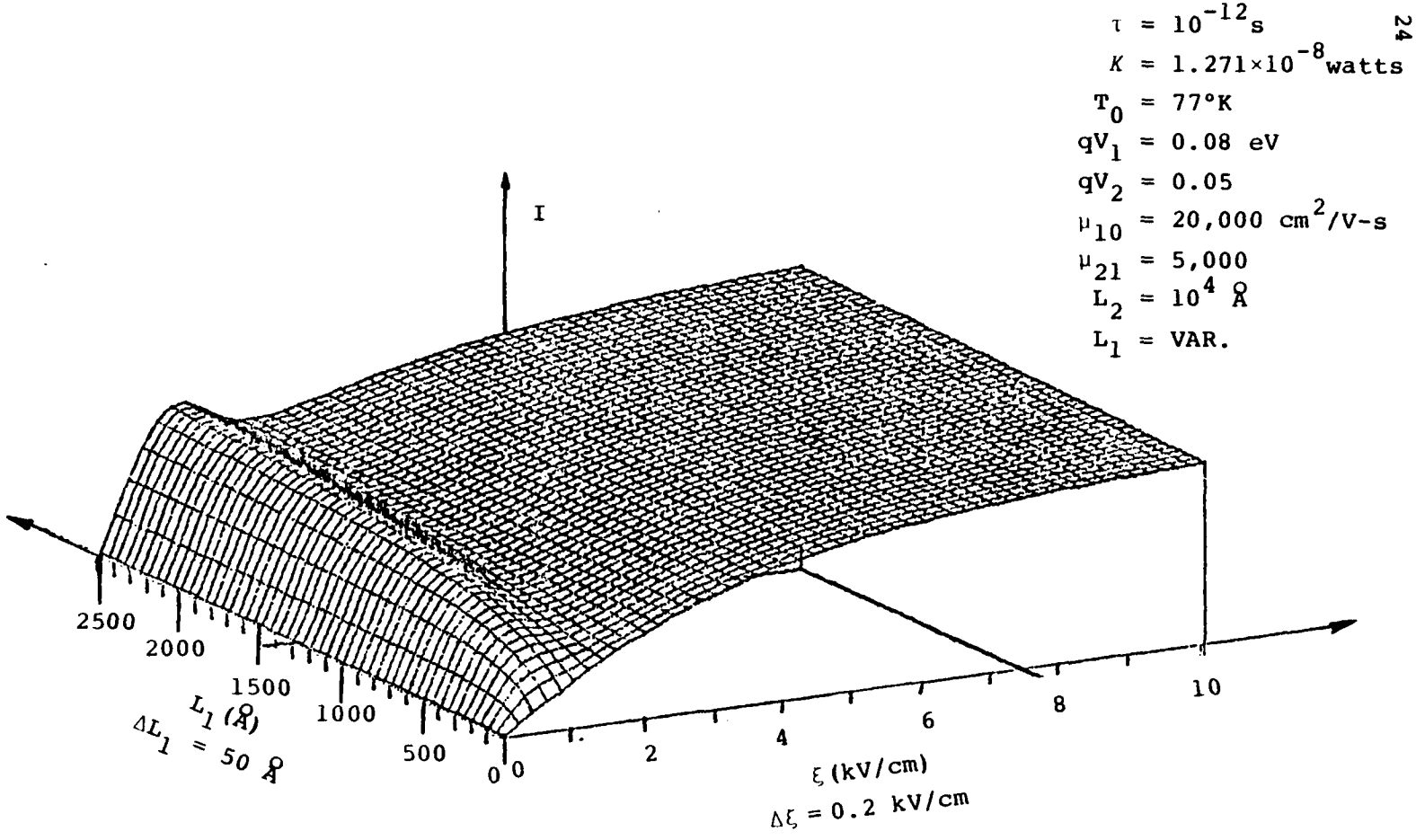

Figure 12. I-ξ curves with GaAs layer thickness L_1 variable.

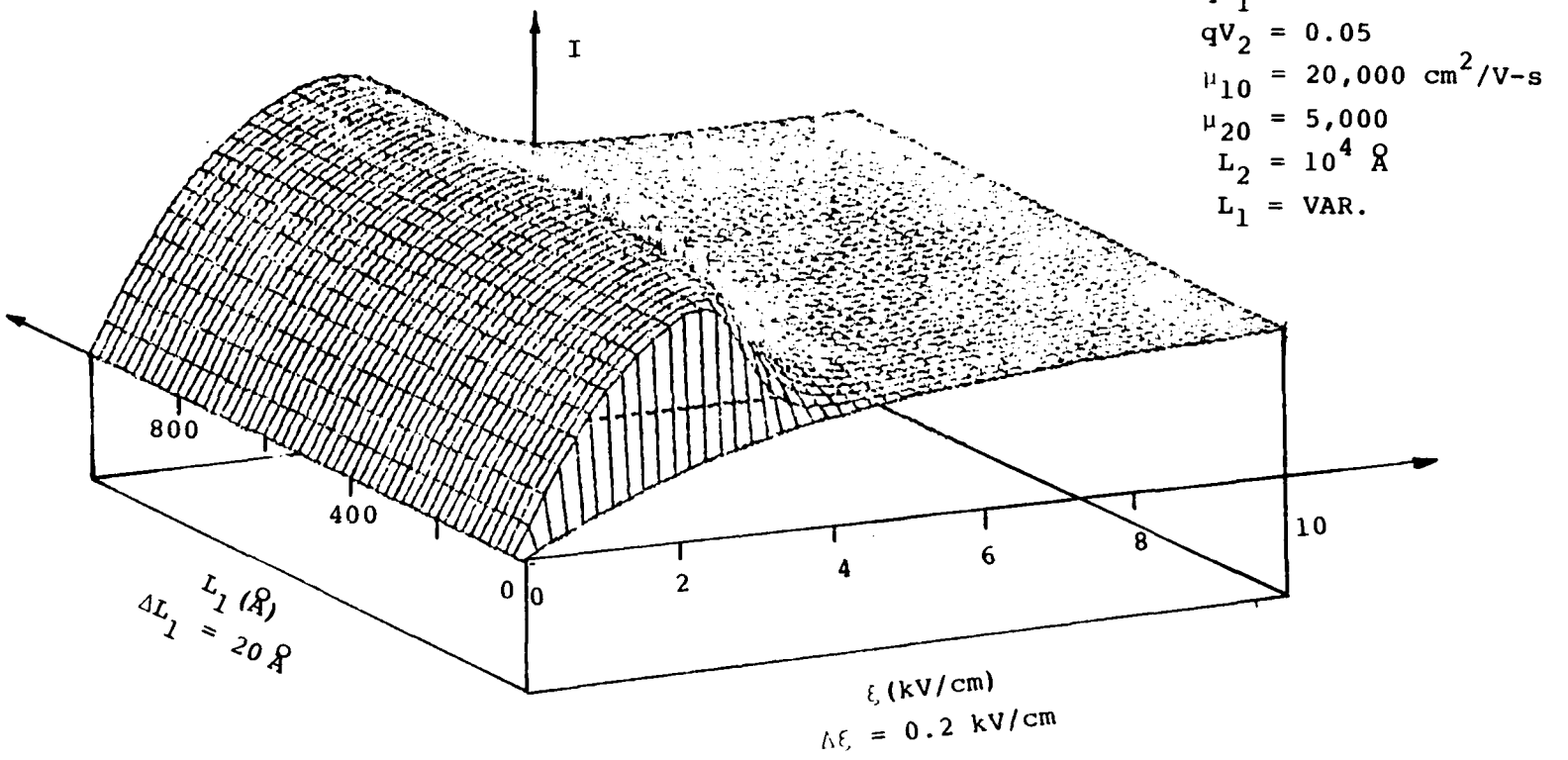

Figure 13. I-$\mathcal{E}$ curves with GaAs layer thickness L_1 variable.

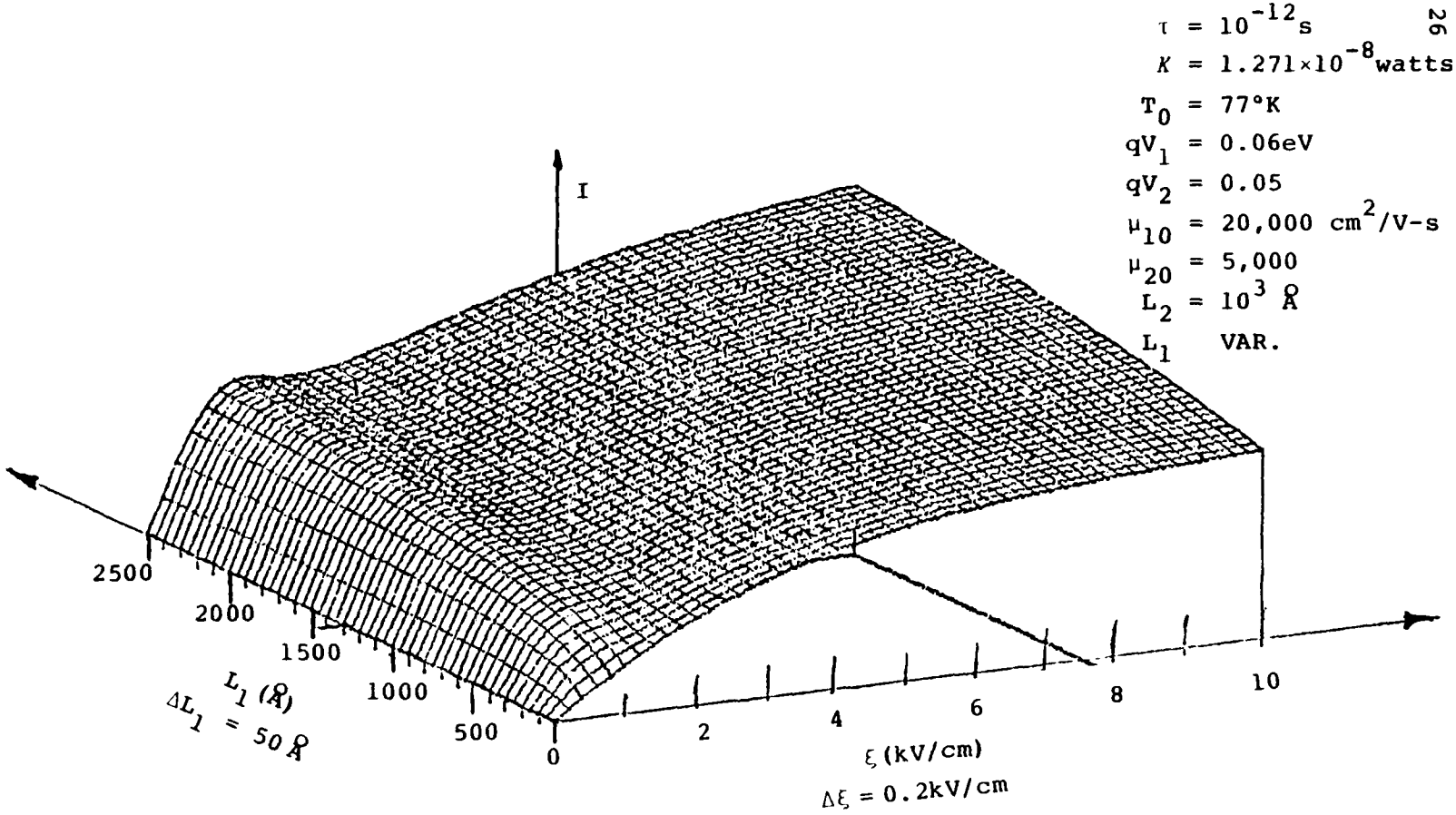

Figure 14. I-ξ curves with GaAs layer thickness L_1 variable.

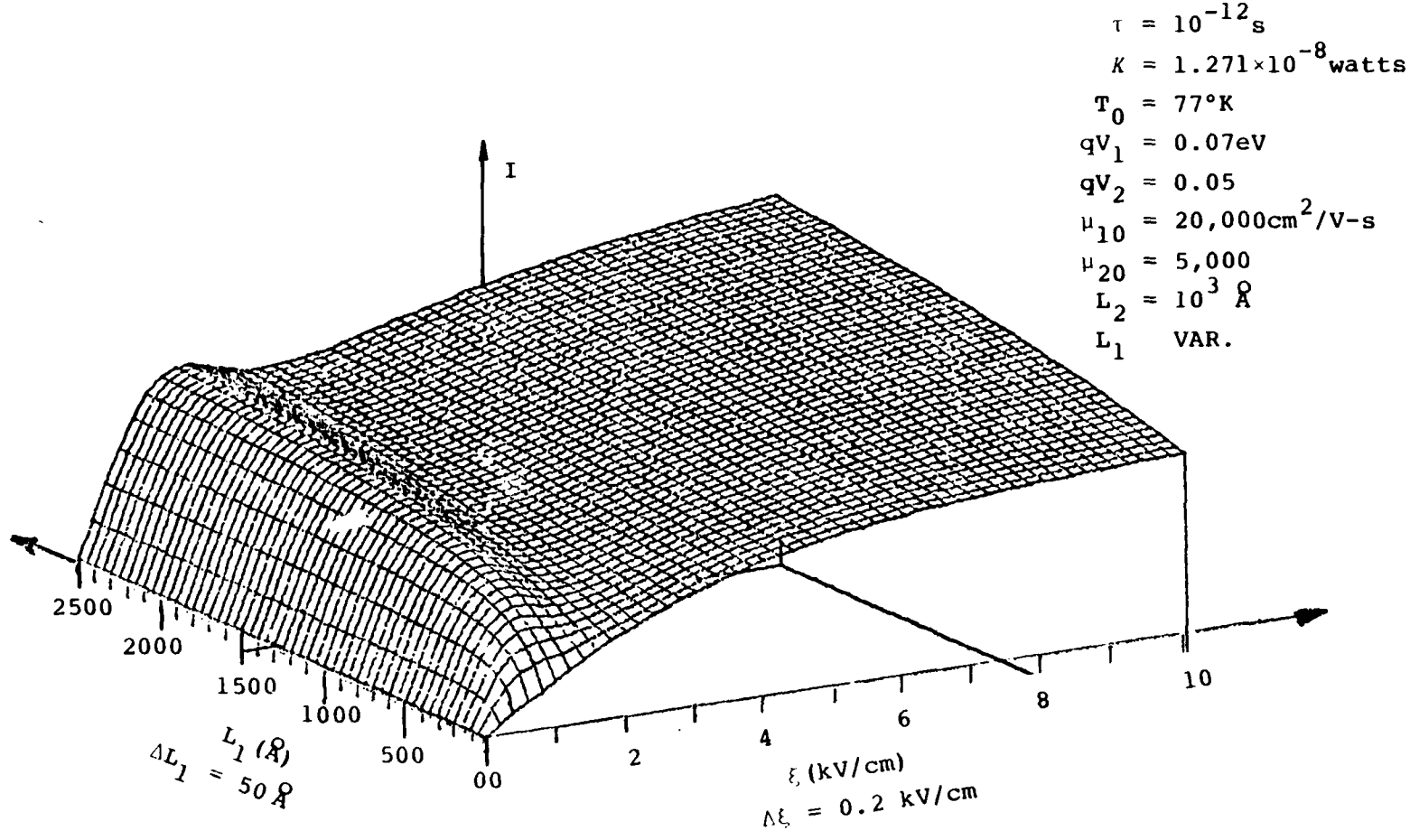

Figure 15. I-$\mathcal{E}$ curves with GaAs layer thickness L_1 variable.

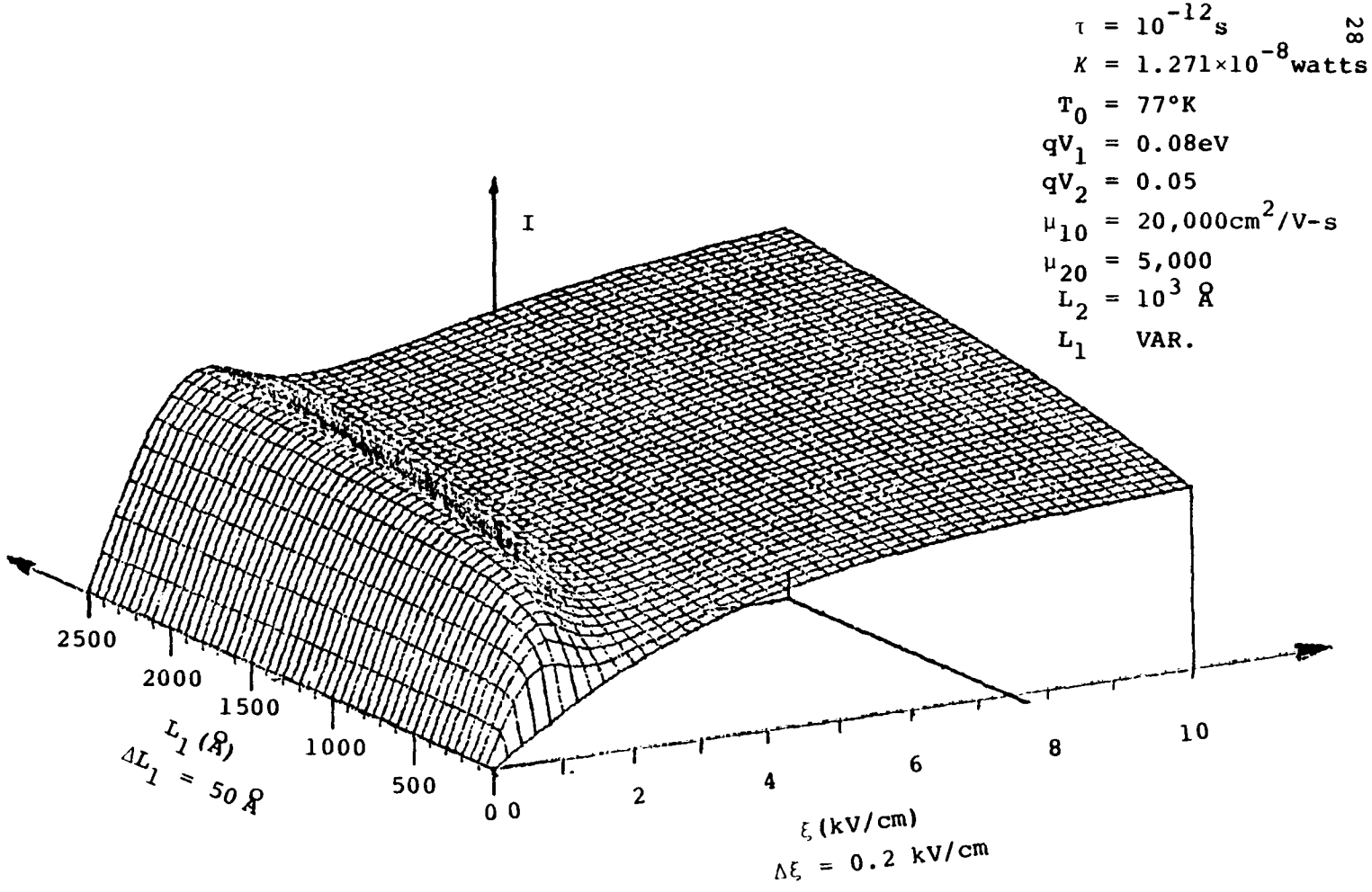

Figure 16. I-ξ curves with GaAs layer thickness L_1 variable.

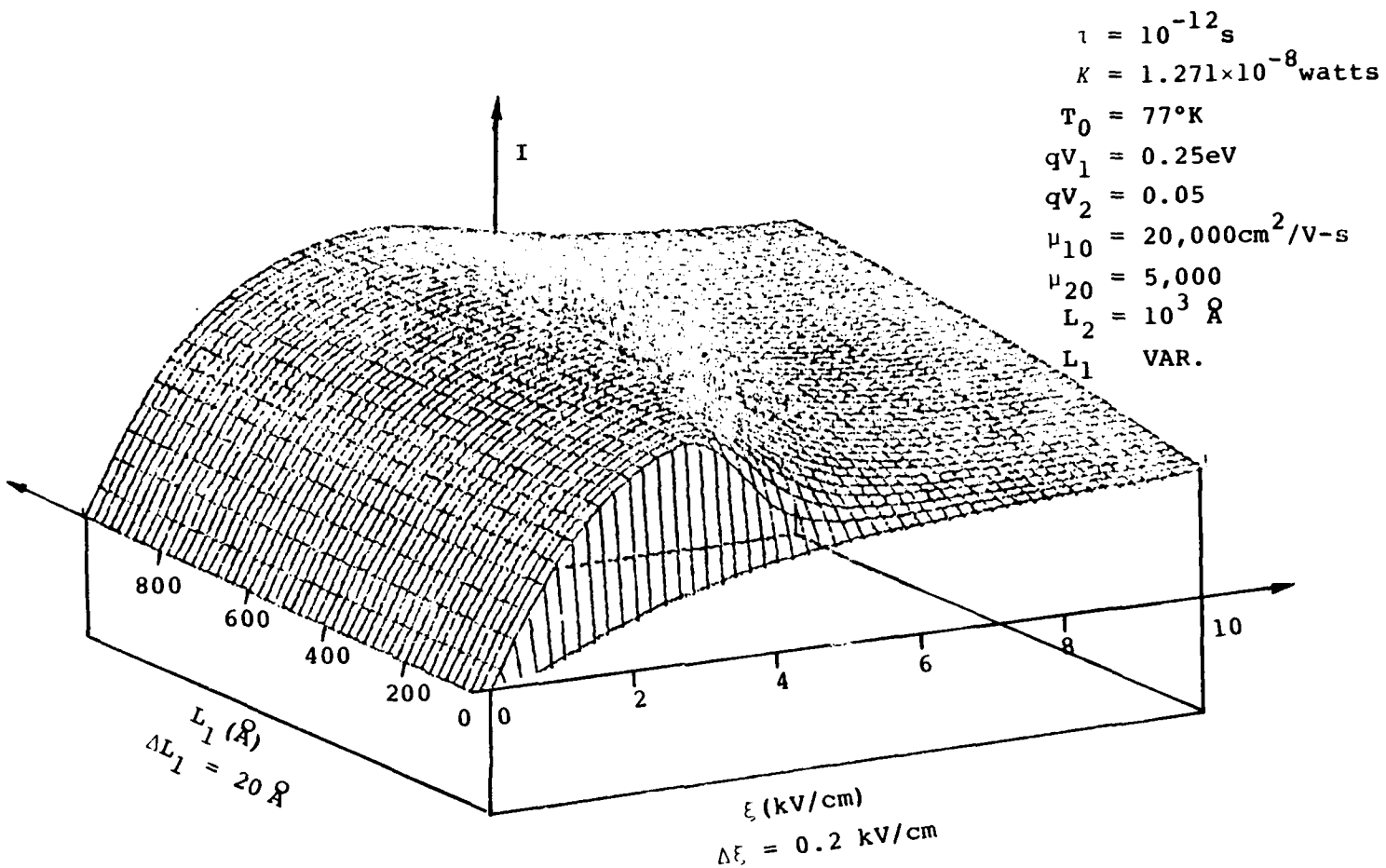

Figure 17. I-ξ curves with GaAs layer thickness L_1 variable.

The curves of Figure 18 with the lattice temperature T_0 variable, indicate that a lower temperature displaces the NDR regions of the I-ξ curves to larger ξ values.

The curves of Figure 19 indicate that larger barrier heights qV_1 displaces the NDR effects to higher field strengths ξ.

The I-ξ curves are consistant with the calculations of H. Shichijo, K. Hess and B. Streetman (Solid State Electronics, 23, 817-822 (1980)),using the Boltzmann equation to analyze the transfer.

7. Conclusions

A GaAs/AlGaAs heterostructure has been made to oscillate for the first time by applying a DC and RF bias parallel to the layered interface. This is a positive proof that a negative differential resistance effect exists for this type of structure. However, it does not definitely prove that the NDR is associated with real space transfer (RST) of electrons. Further experimental work will need to be done to verify RST.

If RST does exist, then the frequency limits of this RSTED oscillator should be at least a factor of 10 larger than any present semiconductor conduction current device. This point also needs to be proven.

The power output should vary as the number of pairs of GaAs/AlGaAs layers. A proof of this point would be very important for high frequency operation above 100 GHz.

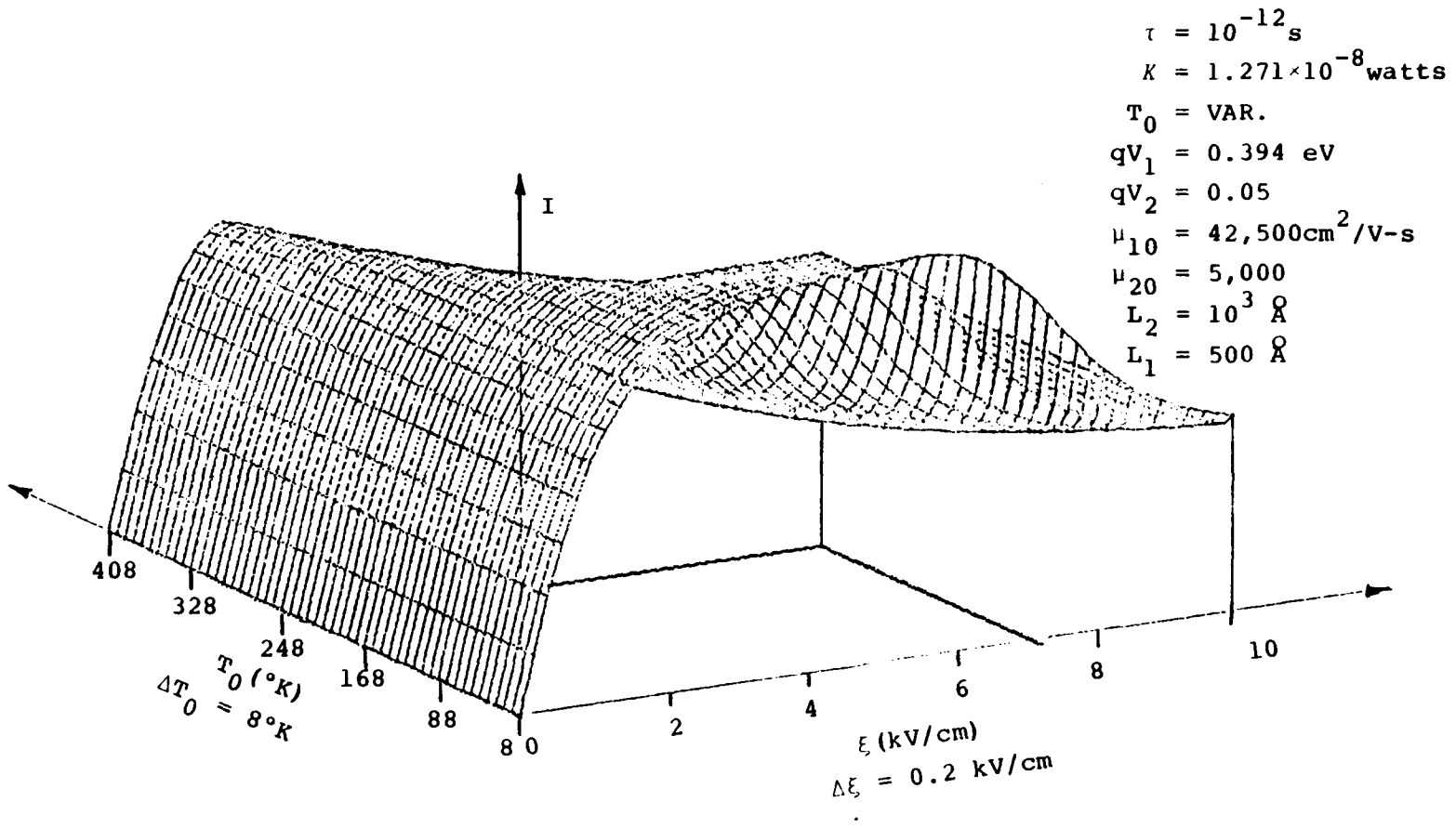

Figure 18. I-ξ curves with lattice temperature T_0 variable.

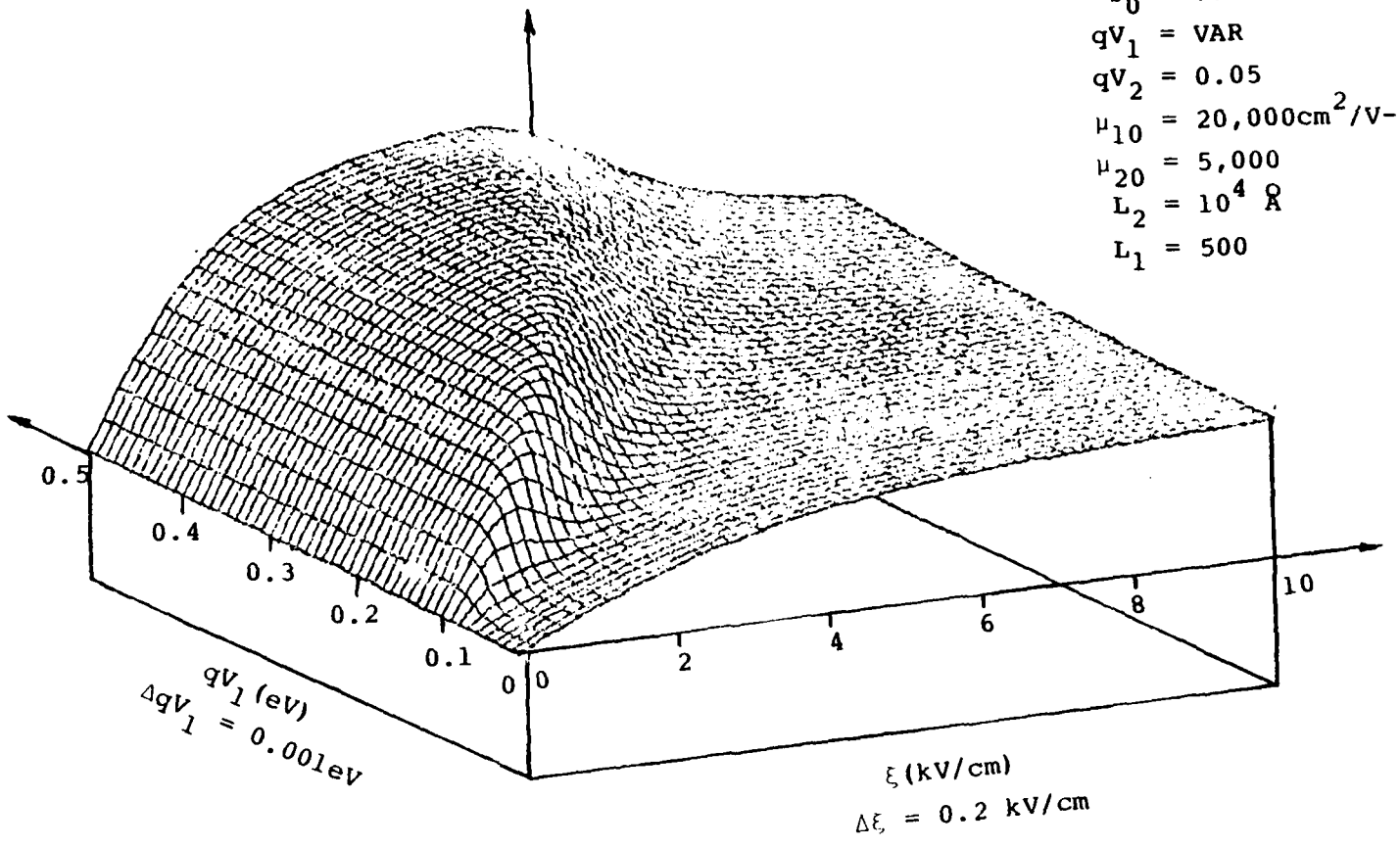

Figure 19. I-V curves with barrier energy qV_1 variable.

A simple thermionic model has been developed to yield a partial roadmap of how to proceed in the design of the heterostructure but detailed data is not yet available to correlate with calculations.

Unfortunately, the lion's share of the effort on this contract was spent on the establishment of basic semiconductor facilities from scratch and learning semiconductor technology. Oscillations were first obtained near the end of the contract period which permitted only a limited study of the oscillator.

8. Acknowledgements

The authors are deeply indebted to Hadis Morkoc and Tim Drummond for supplying the heterostructure wafers used in this work. Numerous discussions with Karl Hess and Ben Streetman on real space transfer were very helpful and the interaction with Mark Keever on I-ξ curves is appreciated. The authors are also indebted to Martin Cooper of Motorola for his gifts of a diamond scriber and probe station and we thank Marty Nisenoff of NRL for his loan of a vacuum deposition system.

It is also a pleasure to acknowledge our interaction with Tom DeTemple, Nick Holonyak, Jr., Greg Stillman, George Anner, Al Cho of BTL, and David Thompson of Rockwell. It would appear semiconductor work requires good contacts of many kinds.

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9. Personnel Associated with Grant

	Percent of Time	Period
Paul D. Coleman Principal Investigator	75% 10% 50% 15%	June 1980/July 1980 August 1980/May 1981 May 1981/July 1981 August 1981/May 1982
Robert Miller Research Assistant	50%	June 1980/January 1981
Jay Freeman Research Assistant	50%	July 1981/May 1982
Mark Wdowik Undergraduate Assistant	Hourly	January 1981/May 1982

APPENDIX A. FABRICATION AND TESTING EQUIPMENT FOR RSTED OSCILLATOR

A-1. LAPPING

MBE grown samples have a coating of either In or Ga metal on the substrate. This is used in MBE processing to adhere the substrate to the heating block and provide a good thermal contact. In our processing steps, however, this metal layer must be removed. The equipment required for this process is:

Lapping Block and Holder (no rotational motion)	"Flat" Glass (coarse lapping)
Glycol Phthalate (white wax)	Alumina Abrasives (15, 8, 1.0, 0.3, 0.06μ)
De-Ionized Water (DI)	Polishing Pads
Hot Plate	The "Four Solutions"

Lapping Procedure

1.1. Sample Mounting

1) Thoroughly clean sample and lapping block by rinsing in the four solutions (trichlor, acetone, methanol, isopropol) and N_2 dry.

2) Place the lapping block on the hot plate and heat to 80°C.

3) Melt a thin layer of white wax over a small area in the center of the lapping block.

4) Place the sample, active layers down, in the white wax and remove the block from the hot plate.

5) As the block and sample are cooling, apply a steady even pressure on two opposite corners of the sample with the wooden ends of two Q-tips until the wax solidifies. White wax tends to bead up and float the sample. This step is necessary to assure plane surfaces.

6) Scrub the lapping block holder in soap and water with a toothbrush, dry, then rinse in the four solutions and N_2 dry.

7) Insert the lapping block into the holder. It may be necessary to wet the block in DI to prevent binding between the block and holder.

1.2. Coarse Lapping

1) Clean the "flat" lapping glass with soap and water to remove any debris that may have accumulated. Rinse first in tap water then in DI. Do not dry.

2) Apply 15μ Centriforce Abrasive to the glass.

3) Gently place the lapping assembly on the glass, with the block slightly recessed in the holder so the sample is not making contact with the glass. Start a figure-8 motion with the assembly and carefully lower the sample to contact the plate.

4) Continue the figure-8 motion and rotate the assembly in the process. Do not apply any force, the weight of the lapping block will be enough.

5) When the metal layer has been removed, remove the block from the assembly and rinse thoroughly with DI to remove all of the abrasive.

6) Repeat steps 1.1.6, 1.1.7, and 1.2.1-4 using 8μ Centriforce Abrasive.

7) Inspect under a microscope to see if the deep grooves from the 15 μ abrasive have been removed.

8) Clean and store the lapping glass and clean (1.16, 7) the lapping assembly to remove all 8μ abrasive.

1.3. Polishing

Three polishing discs have been prepared for exclusive use with 1.0, 0.3, 0.06μ alumina abrasives. These are flat circular discs ½" thick with polishing pads mounted on top. The polishing procedure is the same as that for coarse lapping with the exception of the polishing plate cleaning. Soap may become trapped in the pads so only a DI rinse is used. To determine when to move down to the next size abrasive, one simply inspects the sample under a

microscope to see if all the deep scars from the previous abrasive have been removed.

Removal of the wafer from the lapping block is accomplished by suspending the waxen end of the lapping block in a beaker of hot acetone. The acetone will completely dissolve the white wax and free the sample from the block. The sample should not be forced off of the block, scratching of the very thin active layers may result.

1.4. Notes

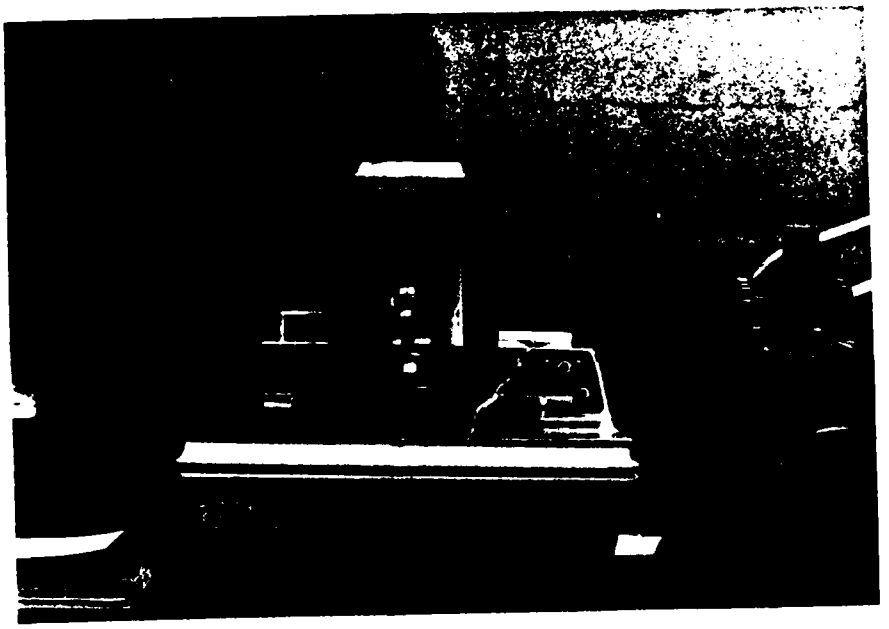
1) To prevent damage to the edges of the sample, due to either "grabbing" between the lapping plate and the sample or play between the block and holder, one should wax three or four pieces of "junk" GaAs in a symmetric pattern about the good sample.

2) To obtain a beval cross section the above lapping procedure may be used with only a few modifications. A standard procedure would be to use a lapping block with a 1° bevel.[1] Protective pieces of GaAs are placed on the leading and trailing edges. Starting with 1.0 abrasive the sample is lapped until 1/3 of the surface has been removed. In this case the lapping motion is to and fro along the leading edge, no rotation. A finishing polish of 0.3 alumina uses full-strength Clorox as the medium. Clorox selectively etches and stains the GaAs/AlGaAs layers. Examination under a microscope shows the defined layers. An alternate approach to the 1° bevel lapping block, if white wax is used, would be to apply pressure to the two adjacent corners of the trailing edge while the wax is cooling. The leading edge will tend to float on the wax yielding a 1-2° bevel.

A-2. CLEAVING AND DICING

Sample scribing is performed on a TEMPRESS 17` 10A automatic diamond scriber donated by the Motorola Corporation. This system features four modes of operation with indexing ranges from 0.0005" to 0.1". The vacuum chuck is removeable so that an assortment of chucks, with various hole patterns, may be incorporated

to accommodate irregular sample sizes. The vacuum state permits small (theta) rotations for wafer alignment and rotations of 90° and 120° for dicing scribes. Scribing pressure and height adjustment controls are located on the slide assembly, which houses the scribing tool, and are easily accessible. The 20X B&L microscope with alignment cross-hairs permits easy wafer alignment and provides excellent vision of the scribes. Mode selection is controlled by two switches; travel-index-normal (upper right), and the normal-ram hold-ram (lower right). With the ram switch in the normal position and the mode switch in the travel position the vacuum chuck will travel either right or left while the actuate switch (momentary contact) is held in the respective direction. In the index mode the chuck will travel the distance set by the thumbwheel switches. Again, the direction in which the actuate switch is depressed determines the direction of travel.



When the ram switch is placed in the ram position the slide/tool assembly will begin its scribing motion, without indexing, and continue until the switch is moved to the ram-hold position. This abruptly stops the scribing motion regardless of the slide assembly's position. With both mode switches in the normal position, the scriber will begin an index-scribe cycle when the actuate switch is hit. However, the indexing direction is not determined by the way the actuate switch is flipped, but, by the angle of rotation of the vacuum chuck. If referenced at 0°, the scribing motion will be from left to right. A 90° or 120° rotation will cause indexing from right to left. Indexing distances for left to right or right to left are determined by the left and right thumbwheel switch assemblies, respectively. To halt the index-scribe cycle, flip the ram switch to the ram hold position.

Cleaving Procedure

2.1. Loading and Calibrating

1) Remove the vacuum chuck, rinse in four solutions and N_2 dry.

2) Rinse both the good and "junk" samples from the same lapping in the four solutions. The "junk" samples will be used to determine the scribing height and pressure.

3) Wipe off the lip that the vacuum chuck rests on with a cleam Kimwipe tissue.

4) Spread a thin coating of Dow Corning vacuum grease around the lip to assure a good vacuum seal, then replace the chuck.

5) Place the "junk" sample upon the chuck and turn on the Master switch. Using tweezers, "roughly" align the sample with the cross-hairs.

6) Energize the vacuum pump and turn on the vacuum switch. Make sure there is a good seal between the sample and the chuck.

7) Using the theta adjust the index mode, align the sample edge with the cross-hairs.

8) Index the chuck 10 mils.

9) Raise the height adjust to its maximum setting and set the pressure adjust to zero.

10) Place the ram switch in the ram position and let the tool make one or two passes before moving the switch to ram hold. Watch to see if the tool contacts the wafer.

11) Lower the tool height one division and repeat the above. Continue this procedure until the tool just makes contact with the wafer.

12) Now raise the tool so it's just above the wafer surface.

13) Index the chuck 10 mils and begin the lower-ram routine until the faintest scribe is visible. The tool height is now set.

14) Index the chuck 30 mils and increase the scribing pressure by 5 g.

15) Make a single scribe across the sample and note the amount of surface damage. (Keep a record).

16) Repeat 2.1.14, 15 until the surface damage becomes intolerable.

2.2. Cleaving

1) Turn off the vacuum switch and transfer the sample to a stack of two or three folded Kimwipe tissues. Place the sample scribed side down.

2) Lay another clean Kimwipe over the back of the sample.

3) Using a pencil type diamond scribe, and staring with the last scribe (greatest pressure), apply a gentle pressure to the sample directly above the scribe. The sample should easily cleave along the scribe.

4) Noting the ease of cleaving, work back to the first scribe.

5) Determine the optimum scribing pressure for this sample thickness. This is usually a trade-off between surface damage and cleaving ease. For scribes to the active layers you would want

to minimize surface damage, whereas, for substrate scribes a little more damage is tolerable.

6) Adjust the scribing pressure to that value and record the scribing height and pressure for future use.

7) Place the good sample on the chuck, align, and begin scribing in either the normal or manual (as in 2.1.14,15) mode.

2.3. Cleaving Notes

1) There are basically three methods which we use for sample cleaving. The first, as described in section 2.2, requires a direct pressure opposite the scribe. A second method[2] for samples 100 μm or less performs the cleaving by placing the scribed samples in an ultrasonic bath. In the third method the sample is lapped, cleaved side up, to a thin metal sheet. By flexing the sheet you can cause the sample to cleave along the scribes.

2) We would prefer to only scribe the wafers on the substrate side while keeping the active layers away from the chuck to prevent scratching them. This may be accomplished by either waxing the sample to a thin stainless steel sheet or by encapsulating the active layers in Si_3N_4. Waxing the sample to a steel sheet has the advantage of permitting you to use a vacuum chuck with a larger hole pattern which gives a better seal between chuck and sample.

A-3. EVAPORATION SYSTEM

Metalization for ohmic contacts to the GaAs-AlGaas heterostructures is accomplished by evaporating thin films of Au-Ge eutectic, Ni, and Au onto the samples in a very high vacuum. The vacuum system has been provided by the Department of the Navy and is manufactured by Vacuum Industries, Inc. This system has a variety of features which provide easy operation and require a strict maintenance schedule.

The pumping system consists of three pumps, two mechanical and a N.R.C. Model NHS6 diffusion pump. The diffusion pump has a 7" I.D. body which may obtain a maximum pumping speed of 1500

L/sec for air. One of the mechanical pumps is used strictly to hold the foreline pressure on the diffusion pump below 100 microns at all times. This is a Welch Duo Seal Model R1403 pump with a maximum speed of 100 L/min. and ultimate vacuum of 5 microns. The other mechanical pump, an Edwards ED660 (660 L/min., ult. vac. 0.1 to 1.0 micron) is switched within the system to either assist the holding pump or rough the bell jar to a pressure less than 50 microns. Under present operating conditions the maximum forepressure is typically 45 microns and the ultimate blank-off for the bell jar is $5\text{-}8\times10^{-7}$ torr.

The foreline, roughing, hold, and high vacuum valves are all pneumatically operated requiring 60 to 80 p.s.i. of either compressed air or nitrogen. The mechanical pump vents are Tomco normally two-way solenoid valves. These are wired in parallel with the pump motors so they are closed when the pumps are energized and automatically open to vent the pumps when they are de-energized. The bell jar vent is also a Tomco two-way solenoid valve but normally closed (see Fig. 1).

The system may be placed in three different modes of operation. These are the Auto-Vent, Hand (manual), and Auto modes. In the Auto-Vent mode all the valves are closed initially. When the roughing and holding pumps are energized the pump vents will close and the hold valve will open. The Auto-Vent mode is also used in the system shutdown as a safety precaution to assure that the high vacuum, vent, rough, and foreline valves are closed before the mechanical pumps are de-energized and vented. In the Hand mode one may control the valve opening and closing sequences by the key lock switches on the control panel. When evacuating the bell jar in the Auto mode one places all the key lock switches in the Auto position (assuming the mechanical pumps are running and the diffusion pump is hot), sets the high vacuum cross-over to the appropriate pressure, then switches the mode selector to the Auto position. The system will automatically cycle through

the valve sequences and evacuate the bell jar. However, the cross-over control on our system is not operational. Thus, until we receive the replacement parts, the system shall be operated in the manual, or "hand" mode. The following are the system start, bell jar evacuation, return to stand-by condition, and complete system shutdown procedures.

3.1. System Start Procedure

1) Check to make sure the key lock switches for the foreline, roughing, vent, and high vacuum valves are all in the off position. Turn the main power switch, water, and compressed nitrogen on. Regulate the nitrogen to 80 p.s.i.

2) Check to make sure the mode selector is in the Auto-Vent position then energize the mechanical pumps.

3) Place the thermocouple selector in the TC2 position. (foreline pressure).

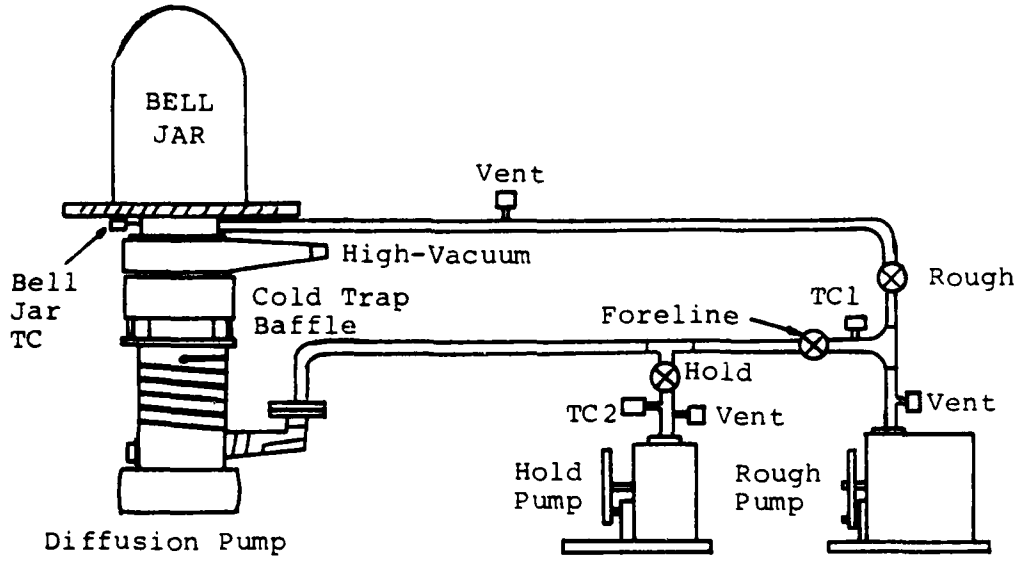


Fig. 1. Schematic representation of the pump and valve configuration.

4) Once the forepressure has reached 100 microns, switch the mode selector to the hand position, then turn the foreline key switch to the hand position.

5) When the pressure has dropped to 50 microns or less, energize the diffusion pump. The diffusion pump will not energize if the mechanical pumps are not running or of the water flow is inadequate.

6) Allow 20 minutes for the diffusion pump to rise to its operating temperature, then fill the liquid nitrogen trap. The system is now in the stand-by condition.

3.2. Evacuating the Bell Jar

1) With the system in the stand-by condition, turn the foreline valve key to the off position. Allow a few seconds to make sure the valve completely seals.

2) Open the roughing valve by placing the switch in the hand position. Monitor the forepressure with TC2 and the chamber pressure with the bell jar thermocouple.

3) When the chamber pressure reaches 50 microns, close the roughing valve, wait a few seconds, then open the foreline valve.

4) Open the high vacuum valve. The bell jar thermocouple should drop to essentially zero within a few seconds.

5) With the range selector set on the 10^{-4} torr range, turn on the ion gauge filament.

6) Push in the current read button below the ion gauge meter. It should read 1.0mA on the lower scale of the ion gauge meter. If it doesn't, adjust the set screw on the back of the chassie.

7) If the pressure is below 1.0×10^{-4} torr, it should be by now, move to the 10^{-5} torr range.

8) Again depress the current read button. For the 10^{-5} torr and lower ranges the current should be 5.0 mA. Adjust by turning the current read button.

9) Select the appropriate range of pressure to monitor the bell jar pressure.

3.3. Venting the Bell Jar

1) Return the ion gauge range selector to the 10^{-4} torr range then turn off the ion gauge filament current.

2) Close the high vacuum valve.

3) After allowing a few seconds for the high vacuum valve to seal open the vent valve. Keep an eye on the forepressure, if the high vacuum valve hasn't sealed correctly the forepressure will begin rising. If this should happen close the vent immediately. After the forepressure has returned to normal, open the high vacuum valve then close it again. Keep doing this until the high vacuum valve seals properly.

4) Once the bell jar has vented completely it may be raised with its hoist. Close the vent valve.

5) The system is once again in the stand-by condition.

3.4. Complete System Shutdown

1) With the system in the stand-by condition turn off the diffusion pump. Allow the pump to cool until it is cool to the touch.

2) If any liquid nitrogen remains in the cold trap it must be boiled off. This may be accomplished by either inserting a small heating coil into the trap or by feeding in warm nitrogen gas.

3) Turn off the water supply to the diffusion pump.

4) Close the foreline valve.

5) Switch to the Auto-Vent mode.

6) De-energize the mechanical pumps and allow them to vent.

7) Turn off the pressurized gas for the valves and the foreline thermocouple power.

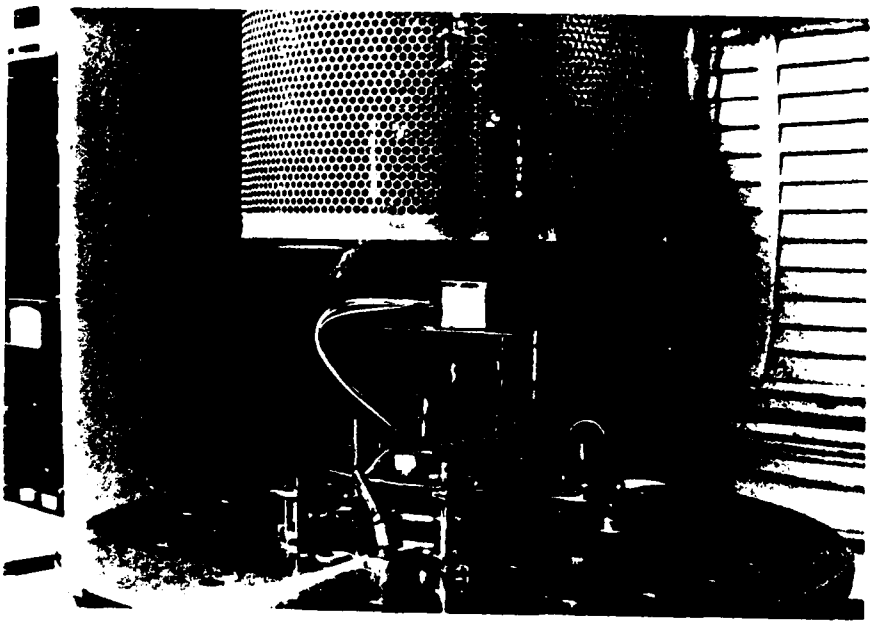
8) Finally, switch off the main power.

The baseplate-bell jar assembly was designed with versatility in mind. The baseplate is 25½" in diameter with a variety of vacuum feedthroughs available for both the 18" Pyrex bell jar and the 24" stainless steel bell jar. Within the O-ring flat for the 18" bell jar there are 12 feedthroughs ranging in size

from 1" to 1-3/4". The feedthroughs and accessories that we received with the system are as listed.

1 - r-f coax feedthrough
1 - 10,000V feedthrough
3 - 400 Amp feedthroughs
2 - ½" dia. rotary feedthroughs
1 - 27 pin T.C. feedthrough
2 - ¼" fluid/gas feedthroughs
1 - 18"×30" Pyrex bell jar with shielding
2 - stainless steel work plates with rigging for evaporation work
3 - blank-offs with tapped holes for work plate feet
1 - d.c. servo motor.

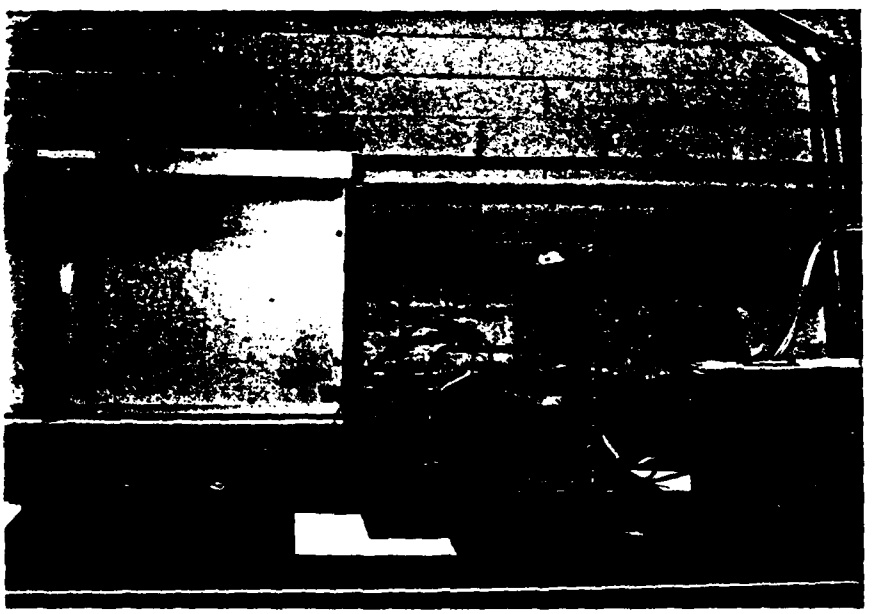
Since our work is concerned mainly with evaporation most of the accessories were removed and blanked off to reduce the number of possible vacuum leak spots. The evaporation rigging provided was designed for tungsten coil type filaments. We are, however, using tablet type metal sources and tungsten evaporation boats. The arrangement has been redesigned, using 8"×3/4"×1/2" Pyrex tubes. A 0-120V Variac coupled with a 5 kW step down transformer delivers the power to the evaporation boats. The thickness of the deposited films is monitored with a Kronos QM-311 thickness monitor



from Veeco Instruments, Inc. The QM-311 has a four-digit numerical thickness display. The Maximum display range is 10 kÅ, 100 kÅ, or 1000 kÅ as selected by the range switches. To program the QM-311 for different materials one uses the density of the material to be evaporated and the geometry of the evaporation configuration to calculate a three-digit number which is set on the thumbwheel switches of the front panel. The water-cooled crystal should be flipped after each evaporation to prolong the crystal's life.

A-4 ALLOYING

Alloying or annealing of the evaporated contacts is performed in a H_2 reducing atmosphere on the strip heater pictured below. The heating element is a 1/16"·1/2"·3" Ni strip with an Iorn-Constantan thermocouple pressure mounted to the bottom center of the strip. A Pyrex bell jar, with a ¼" inlet for the H_2 delivery system, covers the heating strip and contains the reducing atmosphere. Power is supplied by a 120 volt Variac coupled with a 2 kW



step-down transformer. The H_2 delivery consists of bottled H_2 and a liquid nitrogen cold trap (to dry the H_2) with a 100 psi Matheson regulator, Hoke flow valve, and Hoke "Micro Mike" needle valve for gas flow control. Temperature monitoring and graphing are accomplished by the Iorn-Constantan thermocouple connected to a Hewlett-Packard X-Y recorder and Moseley 7001AR autograph.

Alloying Procedure

4.1. System Start and Bakeout

1) With the Hoke flow valve in the off position, fill the cold trap with LN_2, turn on the H_2, and adjust the regulator to 10 psi. Set the needle valve to (8).

2) Open the flow valve and allow the system to purge for three minutes.

3) Turn on the Variac and X-Y recorder. X should be set in the sweep mode at 10 sec/inch and Y should be set to 5 mV/inch. Insert a sheet of graph paper and zero the pen position.

4) Start the record cycle with the pen up. Adjust the Variac so the pen rises to 25 mV and hold for 30 seconds. Return the Variac to zero. When the plotting cycle ends the pen will return to its origin. Assuming room temperature of 20°C, 25 mV corresponds to 437°C.[3]

5) Turn the flow valve off.

4.2. Alloying

1) Remove the bell jar. Place the sample to be alloyed in the center of the strip and replace the bell jar.

2) Open the flow valve and allow the system to purge for three minutes.

3) Start the plotting cycle with the pen down. Turn on the Variac and adjust for a strip temperature of 330°C (19.0 mV), hold for 15 seconds. Further increase the strip temperature to 450°C (25.63 mV) and hold for the recommended alloying time. Return the Variac to zero and shut it off. (The temperatures given are assuming Au-Ge eutectic is being alloyed to GaAs).

4) Once the system has cooled close the flow valve and remove the sample. Replace the bell jar, turn off the H_2, and reopen the flow valve to bleed the pressure from the H_2 line.

A-5 PHOTORESIST PROCESSING EQUIPMENT

To define the small patterns used in etching and metal lifting a minimal amount of photolithograph equipment is necessary. We do not have all of this equipment available in the Electro-Physics Lab at this time, however, we are trying to obtain a workable arrangement. Meanwhile, at least one of the authors would like to thank Professor G. E. Anner for the unlimited use of the undergraduate Micro Electronics Lab. Without this cooperation our research would have been drastically limited.

Basic to the handling of photo-sensitive materials is the proper type of environment. Gold colored lighting and fume hoods are necessities. Room temperature regulation to 65° and an adequate clean air ventilation system are also extremely desirable. The proper equipment for photoresist (PR) application, baking, exposing, development, and subsequent PR removal in this type of environment will allow one to produce fine geometries with relative ease. The following is a brief description of the PR equipment used in our experiments.

5.1. PR Application

The standard method for applying a thin uniform layer of photoresist onto the wafer is to spin it on. This requires a vacuum chuck with a variable speed control. We are using a spinner-chuck assembly manufactured by Headway Research, Inc. The variable speed range is to 10,000 rp with a 30 second duration. Typical operation involves placing the clean dry wafer on the chuck, turning on the vacuum pump, selecting the proper spin speed (roughly 4000 rpm for etchings or 2000 rpm for metal lifts), apply the PR with a syringe, then starting the spinner. After the chuck has stopped spinning, turn off the vacuum pump and the spinner, then remove the wafer.

5.2. Ovens

There are three bakings which are performed in the PR processing. These are: 1) the bake out at 200°C to assure that the wafer is dry before the PR is applied, 2) the prebake at 65°C for Waycoat resist to solidify the PR before placing it onto contact with the mask, and 3) the postbake at 135°C to completely solidify the PR leaving it mostly inert to the wafer etches. We are using two ovens for these processes. A homemade convection oven with a N_2 flow and a Blue-M model OPT-103. The convection oven is used in both the bake out and prebake heatings. The N_2 flow during the prebake is necessary to keep the PR photosensitive. We use the convection oven in the bake out because the N_2 flow during heating will minimize the amount of oxidation to the thin GaAs cap layer. The Blue-M is used for the postbake only if the exposed pattern is to be etched. Otherwise, the convection oven is used. The convection oven temperature range is to 375°C and the Blue-M is to 550°C.

5.3. Masks

The masks that we are currently using in the fabrication procedure were purchased from Towne Laboratories. The sketches below represent the geometries repeated across the mask. The masks were designed for use with a negative type PR which has since proved to be inconvenient. A new set of masks are currently being designed for use with Shipley AZ 1350 positive PR. Mask M1 is used to define a mesa of active layers by defining a pattern that covers the sections of the active layers that are not be be etched. Mask M2 is used in a metal lift process to define the metal contacts. Mask M3 was designed to allow opening contact windows after the entire sample, substrate, active layers, and deposited metal had been encapsulated in Si_3N_4,

SQUARE	I	II	III	IV	V
a (mm)	0.6	0.6	0.6	0.6	0.6
b (μm)	80	120	160	200	240
c (μm)	40	80	120	160	200
d (μm)	100	120	140	160	180

SQUARE	I	II	III	IV	V
a (mm)	0.58	0.58	0.58	0.58	0.58
b (μm)	30	70	110	150	190
c (μm)	20	40	60	80	100
d (μm)	0.20	0.21	0.21	0.21	0.21

SQUARE	a (μm)	b (μm)	c (mm)	d (mm)
I	100	120	0.56	0.56

All "squares" are 1.0mm×2.5mm

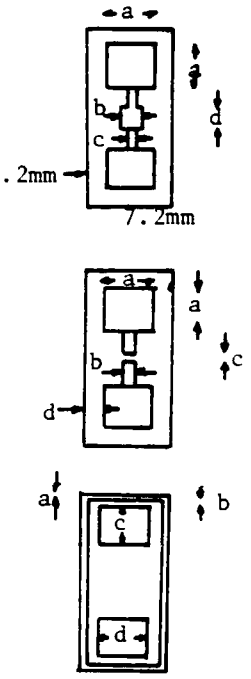
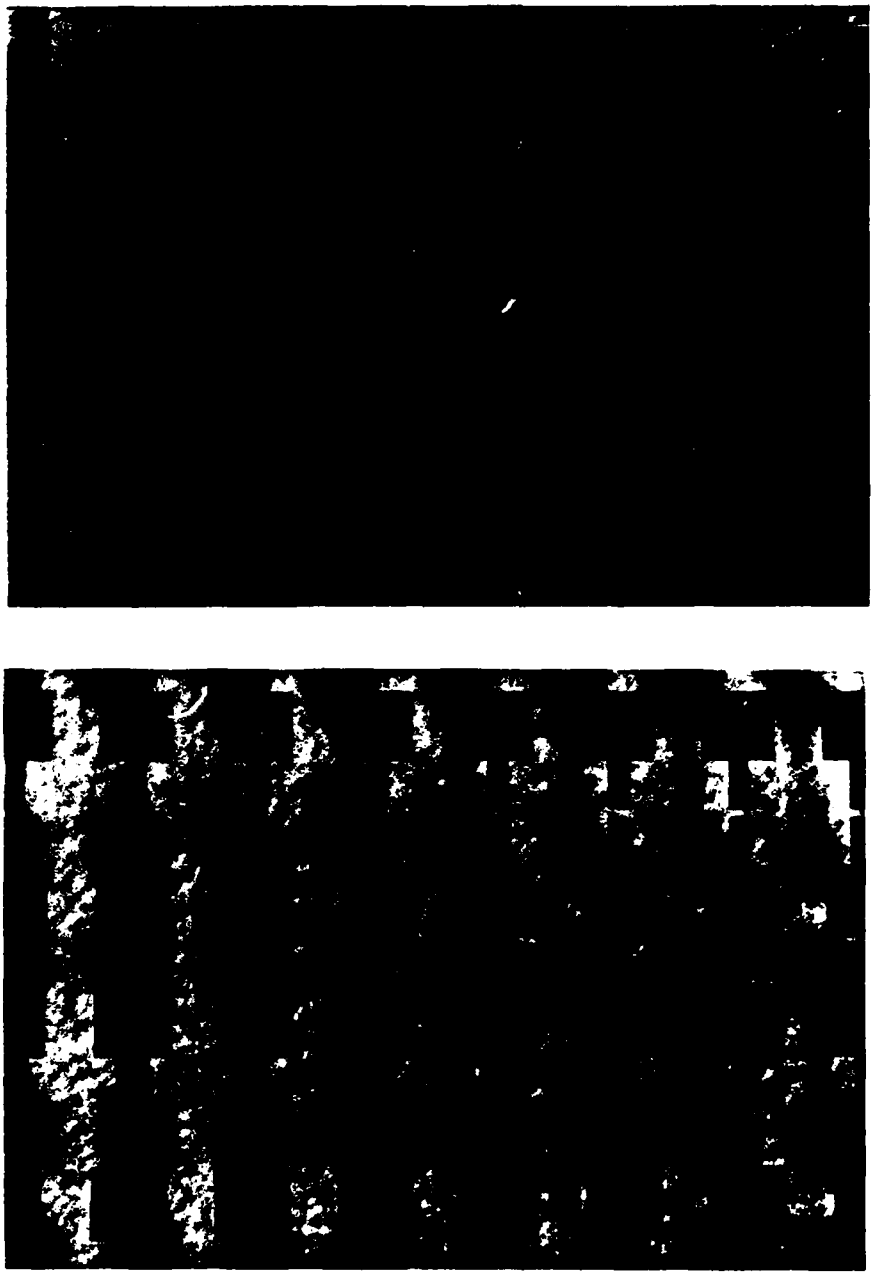


Table 1. Dimensions for each section, or "square" of the repeated pattern for masks M1, M2, and M3.



Photographs of masks M1 (upper) and M2 (lower).

5.4. Mask Aligner

The following excerpt was taken from Professor Anner's EE 344 lab manual. This describes the aligner we are using and the alignment procedure.

The Homemade Mask Aligner

A mask aligner must serve two important functions. First, it must provide means for moving a semiconductor wafer relative to a photomask so that the diffused regions in the wafer may be positioned or aligned with great accuracy relative to the photomask pattern. A microscope system is usually provided so that the alignment may be checked visually.

Secondly, the aligner must provide means for holding the photoresist covered wafer in intimate contact with a photomask during exposure to ultraviolet light. A third ancillary function which may be included is provision of a UV source and system of exposure control.

The homemade aligners have been built to provide these functions. These aligners are completely manual. Therefore, they are good to work with when learning the mechanics of the alignment and exposure process. The homemade aligners are crude in comparison with the commercial aligners, but they have been built for reliability and ease of operation rather than speed and automation. For our purposes these aligners are good, although for finer line geometries the commercial aligners must be used.

Operating Procedures

NOTE: Do not accidentally expose the substrate with the non-gold room lights in transit from the PR room to the aligners.

Alignment:

1. Slide the aligner to the left so that it is not under the microscope. Locate the "fine" x, y, and θ controls and note how they move the wafer platform relative to the outer aligner body to which the mask will be attached. (Unfortunately, some backlash is present on this homemade aligner).

CAUTION: Be careful not to accidentally bump the microscope lenses with the aligner guides when you slide the aligner back and forth.

2. Locate the z control, accessible to your left hand under the wafer platform. This allows the wafer to be moved vertically relative to the mask. Adjust the control so that the wafer carrier is at its lowest position.

3. Handling the substrate by the edges, place it on the foam cushion of one of the alignment jigs.

4. Carefully center the wafer, pattern side up, on the foam cushion with the flat side towards you. Activate the vacuum hold-down so that the wafer is held firmly to the platform.

5. Blow any dust off the sample with N_2 or any empty squeeze bottle.

6. Locate the mask, which is mounted in a metal frame, and gently lower it onto the aligner with the emulsion pattern side down, using the guides provided. Slip weights over the guide pins to aid in holding the mask down securely.

7. Use the z control to bring the wafer close to, but not in contact with the bottom surface of the mask.

8. Observe the alignment of mask and wafer with your naked eye or a magnifying glass. Do not use the microscope here; its field of view is too samll. Adjust the x, y, and θ controls until you have a reasonably good rough alignment. Align the test area first.

9. Locate the coarse X and Y controls. Notice that these move the wafer and mask together as a unit, whereas x, y, θ and z provide relative motion motion between wafer and mask.

10. Slide the aligner to the right and lock it in place under the microscope, being careful not to hit the lens with the guide pins. Choose the lowest power objective on the microscope and turn on the microscope lamp. Lower the objective lens until it is almost in contact with the specimen. Then look through the eyepiece and focus by raising the objective lens from this position.

11. Set X and Y so that you view the pattern near the upper left-hand corner of the mask. You may have to adjust the z control slightly so that both patterns, masks and wafer, are in focus.

NOTE: Never move the x, y, and θ controls when the wafer and mask are in contact; the mask emulsion will be irregpairably damaged.

12. Adjust s, y, and θ for the pattern alignment shown in Fig. 2.1.

13. Set X and Y so you are looking at the lower right hand corner of the mask pattern. TOO BAD -- wafer and mask are probably misaligned. Now -- carefully adjust s, y, and θ to half the misalignment errors.

HINT: Adjust θ first, sweeping Z and Y fully across the wafer. Then use z and y for the final touch-up.

14. Now repeat steps 11, 12 and 13 until you have a satisfactory alignment in the two opposite corners. Do not despair. This is not a 60 second job, especially the first time you do it.

15. Use the X and Y controls so that you can check alignment over the entire wafer surface. Use x, y, and θ for minor touch-ups. When you are satisfied with the overall alignment, proceed.

16. Carefully adjust the z control until the wafer is just in contact with the slide. If you set the mask properly in Step 6 you will see the mask rise slightly. Verify the alignment again. If it is not satisfactory, lower the wafer with the z control and realign.

NOTE: When contact is made both the wafer and mask should rise slightly out of focus. Refocussing will show both patterns simultaneously.

17. Check the alignment with your instructor.

Exposure:

1. When you are sure of alignment, slide the aligner to the left and lock it in place, move the UV source over the sample and center the opening on the bottom side over the pattern.

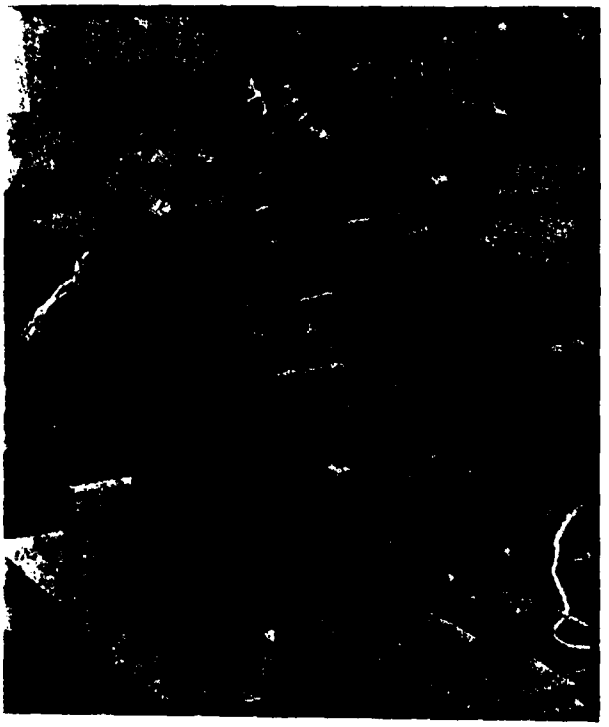
2. Alert the people around you of your impending exposure to avoid accidental damage to their eyes and substrates.

3. Pull out the safety shutter and depress the exposure button on the lamp control bos. Do not hold down the switch. Time is controlled automatically. For Waycoat a 6 second exposure is needed.

4. At the end of the required exposure, push the safety slide back into its closed position and gently side the UV light out of the way.

5. Lower the wafer platform using the Z control, remove the mask, shut off the vacuum valve, and shut off the microscope light.

6. Remove the exposed substrate and retire to the darkroom for the development process.



5.5. Development Station

Development of the exposed PR is an entirely chemical process. Thus, a minimal amount of equipment is necessary. Some beakers to contain the developer and rinses for "dip developing", an atomizer to spray the developer for fine geometries, and a fume hood equipped with a sink are all that is necessary.

Development Procedure

1) Either spray the exposed sample with the appropriate developer or dip them in a beaker of it for the appropriate time. Development time depends on the PR layer thickness and the prebake time.

2) Rinse again by either spraying or dipping in the appropriate rinsing agent.

3) N_2 dry.

4) Check under the mask aligner microscope, gold light, to see if the PR has been completely removed in the selective areas.

5) If necessary repeat the above using a shorter development time to remove all of the PR from the proper areas.

5.6. Microstripping Station

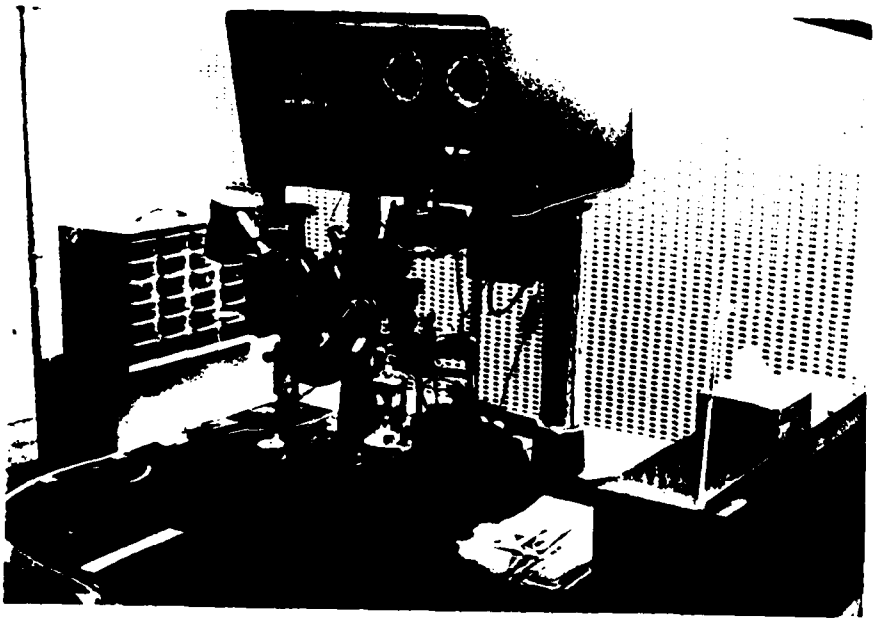
The major advantage of Shipley AZ 1350 is that a postbaked resist layer may be removed by simply rinsing in acetone. For Waycoat I.C. resist, Kodak KPR, and Kodak Microresist 747 a heated etchant is necessary. Thus, a hot plate, teflon beaker, and fume hood are needed to contain the microstripping agent. The microstrip is also much slower and tends to lift the Au in the metal lift procedure.

A-6. WIRE AND DIE BONDS

A Kluckie and Soffa model 420 nail head wire bonder is used for making the die and wire bonds to the devices. The K&S bonder has a variety of features which simplify the bonding process and give reliable bonds. The heat column is pyrometer controlled with a temperature range to 400°C. N_2 forming gas is fed into the heat

column and over the device to provide an inert atmosphere for bonding. The heat column base may be rotated a full 360° and has an inch travel in the x-y plane. The model 420 bonder uses a H_2 flame assembly to cut and ball the Au wire. The capillary assembly may either be heated or cold. We are presently using the cold capillary arrangement with varying results. A heated capillary kit is on order. The capillary, flame-off, and microscope assemblies are all mouned on a single base which travels in the x-y plane via a Chessman micropositioner. This allows capillary movement relative to the header without having to readjust the microscope. Also, uneven ball sizes are prevented. Perpendicular z motion is accomplished by the dice and post bond levers. These finger tip touch level assemblies have presetable timers and adjustable pressure and bonding height controls. The bonding levers when depressed, will lock down at the preset pressure and height for the desired time interval.

The only necessary modification to the bonder was the heat column cap. The cap shipped with the bonder was for use with flatpack type headers, not transistor cases. Thus, a new heat column cap was designed and constructed from machined brass to accommodate a TO-5 transistor header.



There are two bonding processes which are performed on the K&S bonder; the die and wire bonds. In making the die bonds we are using either indium or Au-Ge eutectic as the bonding metal. The indium, while providing a good bond at a low temperature, has the disadvantages of poor wetting, low tensil strength at temperatures necessary to make decent wire bonds, and at temperatures where the tensil strength is sufficient, the wire bonds to the ohmic contacts tend to pull off. The Au-Ge is readily available by scraping off the deposited film from the evaporation rigging chimneys. However, the eutectic temperature is 330°C. The effect of high temperature, if any, on the GaAs surface has not been determined. But, as a matter of caution, we are leaning to the In die bonds. When using Au-Ge die bonds the first wire to pad bond is made simultaneously.

6.1. Indium Die Bonding Procedure

1) Insert a clean (rinsed in four solutions) dry TO-5 transistor header into the heat column cap.

2) Turn on the N_2 gas to provide an inert atmosphere around the heat cap.

3) Turn on the heat column power and set the pyrometer control to 175°C.

4) As the heat column is warming up, place a clean dot of In in the center of the TO-5 header.

5) Once the heat column reaches the operating temperature and the In melts, place the device to be bonded on top of the In dot.

6) Move the sample around with a pair of Teflon-coated tweezers until the In has wetted to the device and the device is laying flat on the header.

7) Set the pyrometer control to 150°C and allow the header-device combination to cool. As the In cools to 150°C, it will solidify to make the die bond.

6.2. Au-Ge Eutectic Die Bonding Procedure

1) Load the header, turn on the N_2, and turn on the heat column as before. The pyrometer control should be set to 350°C.

2) As the heat column is warming up, place a flake of the Au-Ge foil in the center of the header.

3) Set the device on the Au-Ge foil.

4) Position the capillary assembly over one of the bonding pads.

5) Lower the capillary, using the height adjust until the Au wire is in contact with the bonding pad.

6) Increase the bonding pressure until the wire starts to flatten.

7) When the temperature reaches 350°C begin a very slight and gentle scrubbing motion with the Chessman positioner. This is to assure proper wetting between the thin Au-Ge layer and the substrate.

8) Reduce the heat column temperature to 300°C.

9) Reduce the bonding pressure then raise the capillary to its normal position. The first wire bond and the die bond are completed.

6.3. Wire Bonds to Pads

Since we are using the cold capillary assembly and the bonding area is away from the active region, we have found that wedge bonds are easily reproducable and are more difficult to knock off than the typical ball bonds. Thus we have been using the wedge bonding method in our experiments. This, however, may be altered when we receive the heated capillary assembly.

1) After forming the die bond the bonder should be at the proper wire bonding temperature. Make sure the capillary is at the proper height so that when the dice bond lever is depressed it will make contact with the pad before locking in place.

2) Adjust for the proper bonding pressure. This is roughly 4 full turns for 300° bonding, 5 for 150° bonding.

3) Set the bond timers for the proper bonding times; 5 seconds @ 300°C, 12 seconds @ 150°C.

4) Carefully depress the dice bond level until it locks and the timer starts. When the bonding time has elapsed the capillary will automatically raise to the starting height.

6.4. Post Bonds

1) After a pad bond has been completed raise the capillary tip about 1/8" above the top of a post.

2) Using the Chessman positioner move the capillary directly above the post. This should lay the Au wire directly on top of the post.

3) Increase the bonding pressure until the knob begins to tighten.

4) Depress the post bond level until the capillary makes contact with the wire.

5) Apply a slight pressure until you can visually see the Au wire deform.

6) Release the post bond level to allow the capillary to raise. A good post bond should be formed.

7) Raise the capillary about one-half inch.

8) Hit the foot switch for the flame-off. The hydrogen flame should pass the extended wire and cut it forming balls on the severed ends.

6.5. System Shutdown

1) After all pad and wire bonds have been formed remove the device from the heat column with a pair of needle nose pliars and transfer to a nitrogen atmosphere for cooling.

2) If there are no further devices to be bonded turn off the hydrogen flow to the flame off and the power to the heat column.

3) When the heat column has cooled to room temperature, turn off the nitrogen flow and the main power switch.

A-7. LABORATORY CHEMICALS AND MATERIALS

The following is a listing of the chemicals and materials used in our experiments and a brief description of their use

Chemicals: Trichloroethylene, Acetone, Methyl Alcohol, Ethyl alcohol
Use: Cleaning, organic solvents

Chemical: HF (Hydrofloric Acid), selective AlGaAs etch for GaAs/AlGaAs structures
Use: Dissolve Si_3N_4 (and other glasses)

Chemical: HNO_3 (Nitric Acid)
Use: To form aqua regia when mixed with HCL (Au etch)

Chemical: H_2SO_4 (Sulfuric Acid)
Use: Inorganic and metallic solvent

Chemical: HCl (Hydrochloric Acid)
Use: Removes the oxides of GaAs and AlGaAs, also when mixed with HNO_3 forms aqua regia

Chemical: H_2O_2 (Hydrogen peroxide)
Use: Oxidizing agent

Chemical: NH_4OH (Hydrated Ammonia)
Use: Oxidizing agent

Chemical: Deionized Water DI
Use: Solvent, rinsing

Chemical: 3 to 20:1:1 etch, $H_2SO_4:H_2O_2:H_2O$
Use: GaAs and AlGaAs etchant, relatively fast at 3:1:1, slows as H_2SO_4 approaches 20

Chemical: 95%:5% etch, $NH_4OH:H_2O_2$
Use: Selective GaAs etch for GaAs/AlGaAs structures

Chemical: 1:1 etch, Citric acid:H_2O_2
Use: Slow etchant for GaAs, approx. 2500 Å/min.

Chemical: Aqua Regia, 3:1 12M HCL:15M HNO_3
Use: Au etch

Chemical: Au(.88)Ge(.12) eutectic
Use: Metal for ohmic contacts to GaAs, die bonds

Chemical: Ni
Use: Overlayer in contact evaporations to keep Au-Ge from "balling up"

Chemical: Au
Use: Final contact overlayer for wire bonds

Chemical: In
Use: Die bonds

Chemical: Black (Apiezon) Wax
Use: Temporary fastening, protection against etches

Chemical: Glycol phthalate (White Wax)
Use: Temporary fastening

Chemical: Waycoat IC photoresist Type 3
Use: Negative PR

Chemical: Kodak photoresist Type 3
Use: Negative PR

Chemical: Kodak 747 Micro Resist (45 centistokes)
Use: Negative PR

Chemical: Shipley AZ 1350
Use: Positive PR

Chemical: Waycoat Developer
Use: Develops Waycoat PR after U.V. exposure

Chemical: KOR
Use: Develops KPR-3

Chemical: KMR Developer
Use: Develops Kodak 747 PR

Chemical: Shipley Developer
Use: Develops Shipley AZ 1350 PR

Chemical: N-Butyl Acetate
Use: Rinse for Waycoat and KPR-3 PRs

Chemical: KMR Rinse
Use: Rinse for Kodak 747 PR

Chemical: Hunt Microstrip
Use: Stripping agent for Waycoat PR and Kodak 747

Chemical: J-200 Chem. Strip
Use: Stripping agent for KPR-3 PR

A-8. LOW FIELD I-E TESTING

For low electric fields, less than 200 V/cm, electron heating is small in the heterostructure devices so a d.c. field may be used to obtain the I-E characteristic. A schematic presentation of the circuit used for low field testing is shown in Fig. 2. The power supply is adjustable to 50 V and manufactured by Gates Electronics. The meters are Simpson DVMs and the 1 ohm resistor has been measured to be 1.004 ohms. The sample leads may to to a probe station for pre-bond testing, however, the testing is done to the packaged device at either 77°K or 300°K.

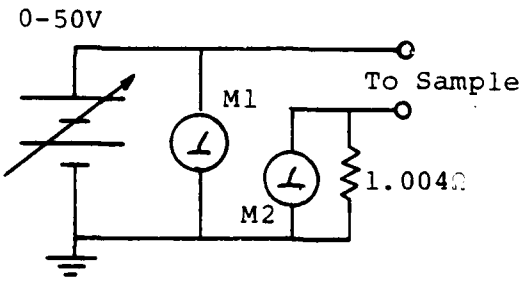


Fig. 2. Circuit schematic.

Testing Procedure

1) Determine the maximum applied voltage for this sample. 200 V/cm × contact spacing.

2) Connect the device to the circuit. 77 or 300°K.

3) Turn on supply (make sure V adjust is at 0) and DVMs.

4) By increasing the voltage take at least five equally spaced readings within the range determined. The voltage across the device is the difference of the M1 and M2 readings. Device current is the M2 reading divided by 1.004 ohms.

5) Return the voltage adjust to zero then switch off the supply meters.

6) Plot the low field I-E curve.

A-9. TESTING EQUIPMENT

The I vs. E-field testing is accomplished by applying a low duty cycle ramp voltage waveform across the series combination of the device and a small sampling resistor. Voltage readings are taken across the series combination and the sampling resistor as shown in Fig. 3. These are fed into two channels of an oscilloscope.

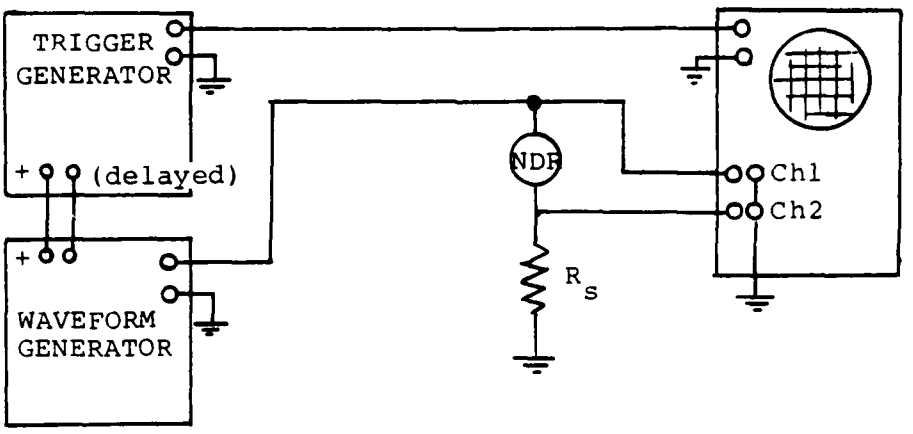


Fig. 3. Block diagram of I vs. E-field circuit.

These two voltage waveforms may either be displayed as functions of time or in an x vs. y mode. The reading from across the sampling resistor is proportional to the current through the series combination. The voltage across the device is almost the same as the applied ramp. However, the actual voltage across the device is the applied voltage less the voltage across the resistor. If the oscilloscope is operated in the x vs. y mode this error is not corrected. The result is a slight distortion of the displayed I vs. E-field plot. The distortion will be an exaggeration of the slopes. This can be used to your advantage in a quick check of the I vs. E-field to see if a negative slope is present even if the magnitude is very small. To obtain the true I vs. E-field plot it is necessary to display both voltages as functions of time then point by point plot the I vs. E-curves with the correction included.

To obtain the low duty cycle ramp waveform with the necessary power requirements the circuit shown in Fig. 4 was designed and constructed.

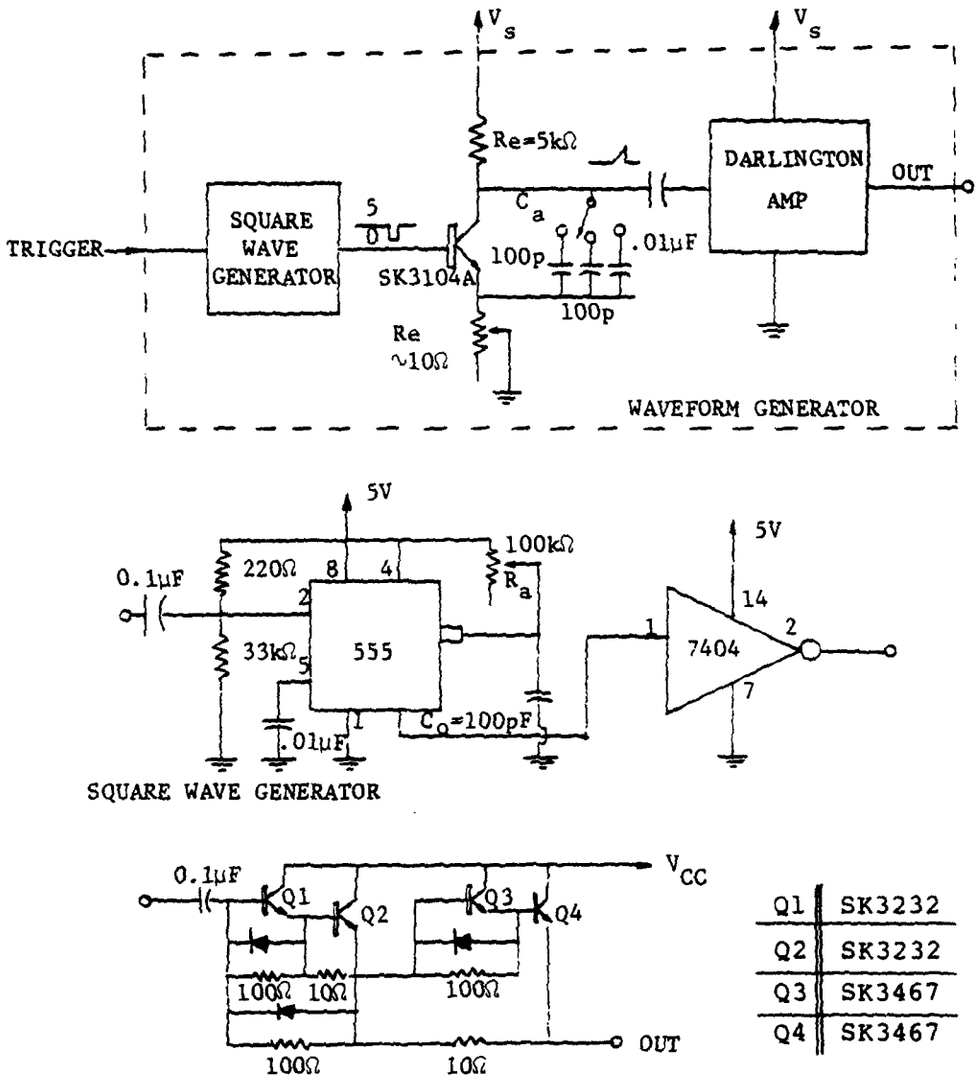


Fig. 4. Darlington amplifier.

The 55 when triggered will produce a 5 V square pulse, the width of which is determined by R_a and C_o.

$$t_o = 1.63\ R_a C_o$$

Here we have made R_a variable so that t_o may be adjustable from 0 μsec to 16.3 μsec. The output of the 555 is inverted and applied to the base of T_1. With the base of T_1 normally at 5 V the transistor will be normally saturated, v_{ce} = 0.1 V. When the 555 is triggered the base voltage of T_1 is clamped to 0 V by the inverter for the duration t_o. This cuts off T_1 and allows the capacitor C_a to begin charging to V_s. The charging rate is determined by the product, $(R_c+R_e)C_a$. If the risetime of the expontential charging is larger than the pulse duration the waveform will be truncated yielding an approximate ramp waveform. The capacitor discharge time constant will be the fall time constant of the transistor.

The output of this stage could be directly coupled to the device-resistor series combination if the impedance of the series combination were 200 kΩ. Unfortunately, the impedance is typically 50 Ω. Thus, a four-stage Darlington combination is used to provide the necessary impedance matching.

The overall performance of the circuit is very good. Of the three C_a settings, the first two, 100 pF and 1000 pF, when used, are capable of delivering 200 V peak to a 50 Ω load with no detectable distortion. However, the circuit, when operated on the third setting, will begin oscillating at 30 V under a 50Ω load.

A-10. PULSE AMPLIFIER

The following pulse amplifier has been designed and constructed to boost the power output of the available commercial pulse generators. A 5 V negative input pulse of 1 microsecond duration is required to trigger the circuit. The output pulse is positive with the maximum voltage determined by the external

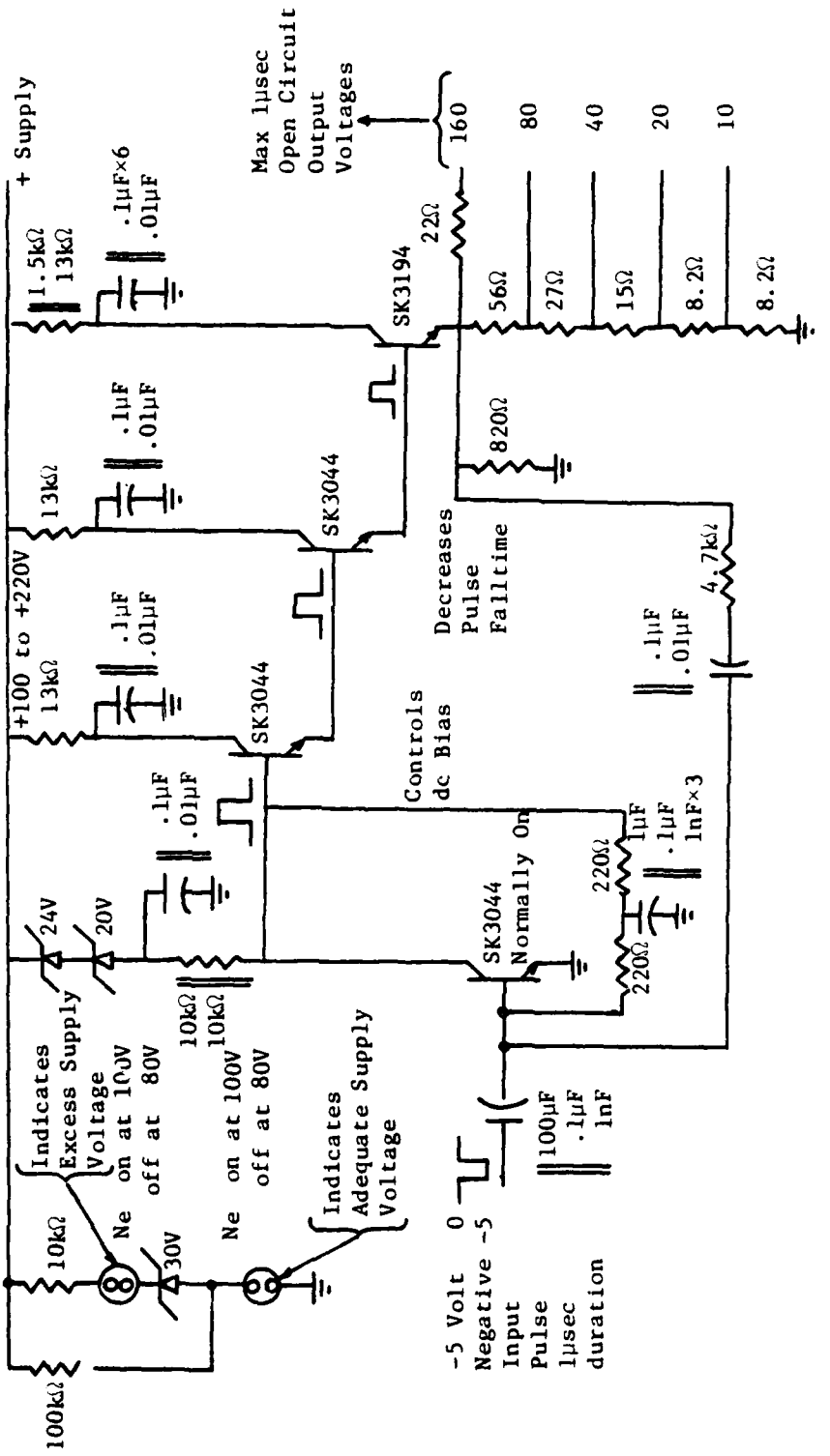


Fig. 5. Pulse amplifier schematic.

supply. A voltage divider on the output allows a wide range of output voltages while only changing the circuit supply voltage over a narrow range. Under worst case operating conditions, the circuit can deliver a 50 V pulse to a 20 ohm load. Pulse duration; 10 microseconds, risetime; 0.4 microseconds, fall time; 0.2 microseconds.

A-11. OSCILLATOR CIRCUIT

The following circuit has been constructed to test the low frequency oscillatory behavior of those devices which display a negative differential resistance. The d.c. biasing is accomplished by the resistive voltage divider. The tank circuit will act as a dc. short and the bypass capacitor, C_2 will act as a dc. open. The small signal ac. equivalent would be the device to be tested in parallel with the series combination of the bypass capacitor and the tank circuit. Thus, the ac. small signal circuit losses are the lead resistances and the inductor resistance, providing the device does have a differential negative resistance. All lead strengths have been kept as short as possible. The tank circuit is tuneable so that we may try to tune the oscillations over a wide range of frequencies. This, with no observations of current spikes, would suggest that Real Space Transfer is the dominant mechanism behind the oscillations and not the "Gunn Effect".

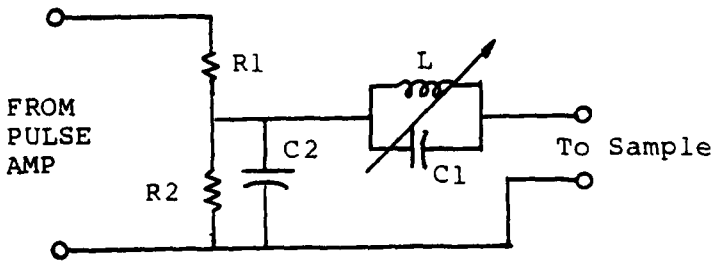


Fig. 6. Basic oscillator circuit schematic.

APPENDIX B. FABRICATION PROCEDURE

B-1. SAMPLE PREPARATION

The sample is first lapped to remove the indium layer on the substrate as in Section A-1. Once the sample has been lapped and rinsed in the four solutions it is then cleaved into appropriate sizes for both types of fabrication procedures. The samples are then rinsed again and dried, then stored until ready for use.

B-2. PLANAR CONTACTS PROCEDURE (PR PROCESSING)

The devices fabricated by this method are generally intended for I-E and low frequency oscillator testing since the geometry is rather awkward for use in microwave cavities.

The second etching, to define the mesa on which the ohmic contacts are made, may not be necessary. Thus, one could skip steps 2.1.1 through 2.3.4 and begin with the second PR spinning. However, by etching the mesa any possible damage to the active layers during dicing is avoided.

2.1. Spin on, Expose and Develop PR

1) Bake out the wafer in the convection oven at 135°C for 20 minutes with the N_2 flow set at 4.

2) Center the wafer on the vacuum chuck of the PR spinner and turn on the vacuum.

3) Cover the surface with PR and let stand for 15 seconds to allow any air bubbles to rise.

4) Spin at 4000 rpm for 30 seconds.

5) Slide the wafer onto a clean piece of filter paper and place in the convection oven. Prebake at 65° for 10 minutes (Waycoat PR) with the N_2 flow at 4.

6) Align the wafer under Mask M1 and expose to ultra-violet light for 10 seconds.

7) Spray the exposed sample with develope for 10 seconds then spray with rinse for another 10 seconds.

8) Dip the sample in developer for 10 seconds then rinse thoroughly and N_2 dry.

9) Inspect the sample under the mask aligner microscope (gold lighting) to see if all of the unexposed PR has been removed. If not, repeat 2.1.6,7 and inspect again.

10) Place the sample in the Blue-M oven and postbake at 135° C for 20 minutes.

2.2. Etching

1) Remove the sample from the Blue-M oven and let cool for roughly 5 minutes.

2) Attach the sample substrate to a glass microscope slide with black wax.

3) Etch the exposed active layers down to the 1 m buffer layer by either immersing in 7:1:1 H_2SO_4:H_2O_2:H_2O for 5 seconds or using the selective etches, HF and 95%:5% NH_4OH:H_2O_2 to remove the layers individually.

4) Quench all etches by immersing in successive DI baths then in flowing DI. N_2 dry.

5) Detach the sample from the slide and place in a beaker of hot trichlor to remove the black wax.

6) Rinse thoroughly in the four solutions and N_2 dry.

2.3. Microstripping

1) Place the wafer in the teflon beacker containing the microstripping agent heated to 120°C.

2) Let stand for 5 to 10 minutes.

3) Remove the sample, rinse thoroughly in methanol isopropyl and N_2 dry.

2.4. Shipley AZ 1350 PR Application

1) Apply AZ 1350 using the same procedure as in 2.1 but use a spinning speed of 2000 rpm for a thicker emulsion.

2) Prebake for 10 minutes in the convection oven with N_2 flowing at 4.

3) Align under Mask M2 and expose for 30 seconds to UV light.

4) Dip develop for 60 seconds then rinse in DI.

5) Inspect (under gold light) and repeat developing if necessary.

6) Do not postbake.

2.5. Metalization

1) Load wafer in evaporation system.

2) Evaporate 2000 Å Au-Ge eutectic, 200 Å Ni, and 2000 Au onto the sample.

3) Break the bell jar vacuum, remove sample and allow to cool.

2.6. Metal Lift

1) Place sample in a beaker of warm acetone.

2) Let stand for 60 seconds then place the beaker in an ultrasonic bath. The PR with metal on top should come off easily.

3) Remove sample from the beaker and rinse in fresh acetone, methanol, and isopropyl, then N_2 dry.

4) Inspect the sample to see if all of the metalization (expect the contacts) has been removed.

5) If some spots remain they may be easily removed by lightly scrubbing the sample with an acetone soaked Q-tip.

6) Rinse the sample in acetone, methanol, isopropyl and N_2 dry.

The sample is now rady for dicing and packaging.

B-3. EDGE FABRICATION

For use in microwave cavities it would be convenient to have the active layers of the device running vertically with the metalization horizontal on the top and bottom edges. Problems arise however when considering the small size of the devices to be handled during processing and the thickness of the layers to be contacted, less than 1 μm. We have, however, been making a few devices of this type geometry from each sample in order to work out some of the technique difficulties.

3.1. Cleaving

In order to keep the applied voltage to the device down to reasonable values we would like to keep the contact spacing

less than 150 μm. (A 150 μm contact spacing requires 30V for a field strength of 2 kV/cm). To accomplish this the samples are lapped to a thickness of 4 to 5 mils then scribed within that range on the Tempress scriber. Cleaving is done in an ultrasonic bath. 4 mil × 4 mil × 1 cm parallelepipeds are the resulting samples to work with.

3.2. Metalization

The samples are loaded into a jig which grips the substrate and cap layer thus leaving one of the cleaved sides exposed. The surfaces in contact with the sample are Pyrex glass and the gripping force is a light spring tension. The cleaved side is slightly recessed from the plane formed by the glass supports forming a shallow well.

The jig is loaded into the evaporation system with attention focussed on the orientation. The jig is place slightly off center from the evaporation boats so that some shadowing will occur. The shadowing is done on the substrate side. This assures that metal will be applied to the thin active layers.

One one side 2000 Å AuGe, 200 Å Ni, and 2000 Å Au is evaporated. This is the side that will be wire bonded. The sample is flipped over then 2000 Å AuGe, 200 Å Ni and another 2000 Å AuGe layer is evaporated. This side is for die bonding.

3.3. Alloying and Packaging

The sample is cleaved into the individual devices before alloying. Individual devices are then placed on TO-5 headers and alloyed as in A-4; this forms the die bond also. After wire bonding and securing a header cap, the devices are ready for testing.

The results have in general been good with this type of fabrication. Contact to the active layers have been missed only once. The biggest problem, other than slow processing, has been the device failure. These devices seem to burn out at field

strengths roughly 1 kV/cm less than the planar fabricated devices. This could be due to rough edges on the metalization (high field points) or dislocations under the contacts induced during alloying as discussed in papers on source-drain burnout in GaAs MESFET's.

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Demonstration of a new oscillator based on real-space transfer in heterojunctions

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A new real-space transfer oscillator is demonstrated in a layered GaAs/*n*AlGaAs heterojunction. A dc bias field, plus the ac oscillating field, is applied parallel to the layer interfaces to modulate the electron transfer from the GaAs layers to the *n*AlGaAs layers. This periodic electron transfer results in the ac current being 180° out of phase with the ac voltage and power being generated. A unique characteristic of this oscillator is that the electron transit times are associated with transverse dimensions and not dimensions between the ohmic contacts which should permit its extension to very high frequencies.

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In this letter it is demonstrated that if a dc plus ac electric field is applied parallel to the layered interface of a heterostructure, a new type of conduction current oscillator making use of real-space transfer has been realized.

The principle of oscillation can be explained with the aid of Fig. 1 which depicts a three-layer GaAs-*n*$Al_xGa_{1-x}As$ heterostructure with a dc and ac bias applied parallel to the layered interface. The applied voltages will cause dc and ac heating of the electrons in the low resistance GaAs layer periodically moving them between the GaAs layer and the high resistance *n*$Al_xGa_{1-x}As$ layers. This will result in the ac current being 180° out of phase with the ac voltage to achieve power generation.

A particularly interesting aspect of this conduction current oscillator is that the electron "transit times" are associated with transverse dimensions of the structure and not distance between the ohmic contacts.[1] Here the GaAs layer can be made quite thin (50–200 Å) so that the hot electrons have a small distance to travel to reach the *n*-type $Al_xGa_{1-x}As$ layers.

The J-ξ current density, electric field) characteristics of these layered GaAs/*n*$Al_xGa_{1-x}As$ structures have been studied by Hess,[1] Shichijo,[2] Keever[3] and colleagues, and the enhanced mobility by Dingle *et al.*[4] and Morkoç and colleagues.[5] These studies confirm the transfer of electrons from their parent donors in the $Al_xGa_{1-x}As$ to the GaAs and support the reverse transfer back to the $Al_xGa_{1-x}As$ by high-field heating of the electrons.

The "three-period" GaAs/*n*$Al_xGa_{1-x}As$ heterostructure used in the experiments is shown in Fig. 2. This structure had an undoped $Al_xGa_{1-x}As$ buffer layer to further enhance the mobility in the GaAs, but it is believed that this is not necessary for the oscillator application.

A tunnel diode rf circuit,[6] shown in Fig. 3, was used to study the oscillator behavior in the 2–25-MHz range for convenience in oscilloscope measurements. The heterostructure was mounted in a transistor header which was placed in liquid nitrogen. Pulsed voltages in the 1–5-μs range at low repetition rates of 50–100 Hz were employed to avoid heating the device appreciably. The heterostructure sample dimensions were 1-mm width with 50-μm metal contact spacing.

An I-V curve of the three-period sample is shown in Fig. 4. It is seen that the current saturates around 10 V and displays a slight negative slope for voltages of 10–25 V.

Oscillator traces of the oscillator behavior and waveforms are displayed in Fig. 5. In (a) and (b), the LC circuit was tuned to 2 MHz while in (c) and (d), the LC circuit was tuned to 25 MHz. As seen in Figs. 5(a) and 5(b), as the pulsed bias voltage is increased, one first sees a small highly damped ringing of the LC circuit at the start of the trace, then as threshold is approached the damping decreases, the ringing increases and in Fig. 5(b) steady-state oscillation is achieved with further increase in bias. The behavior at 25 MHz is identical to that at 2 MHz with the bias voltage near 13 V and the peak rf voltage near 3 V. Increasing the dc bias beyond 13 V did not appreciably increase the peak rf voltages.

These real-space transfer oscillator characteristics are to be contrasted to those of a Gunn oscillator. In the traveling dipole domain mode ($nl > 2 \times 10^{12}$ cm^{-2}) a Gunn oscillator shows little response to circuit tuning as demonstrated for example by Hakki and Knight.[7] Here the real-space

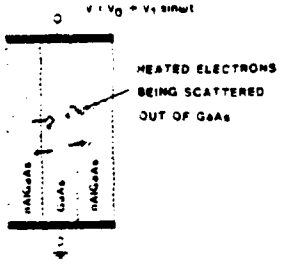

FIG. 1. Periodically heated electrons moving in and out of GaAs layers in heterojunction

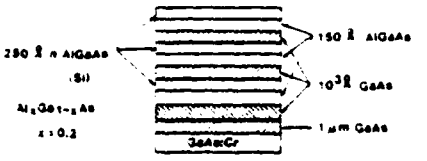

FIG. 2. Three-period GaAs/AlGaAs heterostructure.

transfer oscillator could readily be tuned in the range 2–25 MHz by means of the LC circuit. Increasing the dc drive of the oscillator above threshold did not appreciably increase the power output whereas Hakki demonstrated almost linear dependence of the output with dc input in his Gunn oscillator. Dipole domain formation appears to be prevented by the electrons transferring from the GaAs to the AlGaAs layers. The field threshold for the real-space transfer device is 2 kV/cm which is somewhat less than that for a Gunn device.

The electron mobility in these multiple-period $Al_xGa_{1-x}As$/GaAs modulation doped heterojunction structures shows saturation effects[1] beginning at very low electric fields ($\mathcal{E} < 0.2$ kV/cm) at lattice temperatures below 170 °K. Hot-electron effects in bulk GaAs are not usually observed below the Gunn threshold of about 3 kV/cm.

Shining light on the sample immediately stopped the oscillations and after removal of the light, the order of a half-minute was required for the oscillations to reappear at 77 °K.

This behavior is consistent with the persistent photoconductive effect (PPC) reported by Störmer *et al.*[9] in 1974. In a recent paper Störmer and colleagues[10] have used PPC to vary the areal electron density in GaAs–AlGaAs heterojunctions by nearly a factor of 3. The oscillator demonstrated here is sensitive to how the DX centers[11] in the AlGaAs are ionized. Thus one can also rule out any oscillation phenomena due to deep levels whose frequency is dependent only on the deep level density.[12]

The PPC effect on the oscillator characteristics appears to be a different photoeffect than that seen by Keever *et al.*[13] in their I-$\mathcal{E}$ studies on heterostructures.

Shichijo *et al.*[2] have analyzed the problem of thermionic emission in the GaAs-$Al_xGa_{1-x}As$ heterostructure for the case of steady state using the Boltzmann equation. An oversimplified model can be used to display some of the key features of the oscillator behavior.

First, a power balance for the electron heating is assumed in the form

$$\frac{\partial}{\partial t}\left(\frac{3n}{2}(kT - kT_0)\right) - \frac{3n}{2\tau}(kT - kT_0) = qnv_{sat}\mathcal{E}, \quad (1)$$

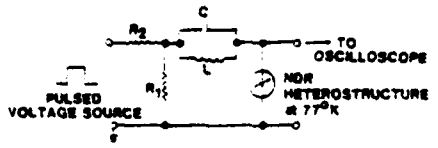

FIG. 3. NDR structure oscillator circuit.

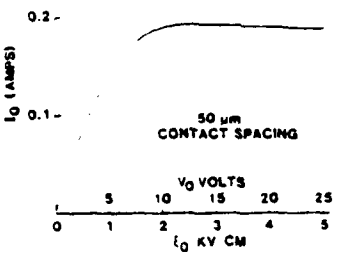

FIG. 4. I-V characteristics of GaAs/AlGaAs heterostructure NDR device.

where heat flow of the hot electrons is implied in $\tau = \tau_E$.

Here n is the electron density, τ the energy relaxation time, v_{sat} the saturation velocity, and $\mathcal{E} = \mathcal{E}_0 - \mathcal{E}_1 e^{j\omega t}$ is the electric field. The steady-state solution is seen to be

$$kT = kT_0 + \tfrac{1}{3}qv_{sat}\tau\mathcal{E}_0 - \frac{2qv_{sat}\tau\mathcal{E}_1}{3(1 - j\omega\tau)}e^{j\omega t}$$
$$= A - Be^{j\omega t}, \quad (2)$$

i.e., the electron temperature is periodically modulated by the ac electric field about some dc value larger than T_0. This temperature modulation of the electrons in the GaAs layer will cause them to move in real space between the GaAs layer and the n-$Al_xGa_{1-x}As$ layers.

These hot electrons in the GaAs will need to surmount an energy barrier ΔE to reach the n-type $Al_xGa_{1-x}As$. Assuming a Maxwell distribution, the fraction F with sufficient energy is readily seen to be

$$F = 1 - \frac{2}{\sqrt{\pi}}\int_0^{\sqrt{\Delta E/kT}} e^{-x^2}dx \cong 1 - \left(\frac{E}{kT}\right)^{\frac{1}{2}}, \quad (3)$$

for $\sqrt{\Delta E/kT} < 1$.

Assuming half of these electrons are transferred, the resulting current for the GaAs layer is

$$J = qv_{sat}n\left(1 - \frac{E}{2}\right) \cong \frac{qv_{sat}n}{2}\left(1 - \left(\frac{\Delta E}{kT}\right)^{\frac{1}{2}}\right). \quad (4)$$

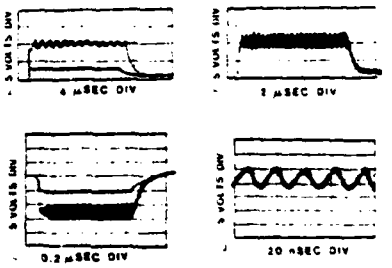

FIG. 5. Oscillation behavior of a NDR GaAs/nAlGaAs heterostructure. (a) Below and near oscillation threshold; (b) above oscillation threshold, $f \cong 2$ MHz; (c) below and above oscillation threshold; (d) expanded view of voltage waveform, $f \cong 23$ MHz.

Substituting for κT from Eq. (2), assuming $B \ll A$, the current J becomes

$$J \cong \frac{qv_{sat}n}{2}\left\{\left[1-\left(\frac{\Delta E}{A}\right)^{1/2}\right]-\left(\frac{\Delta E}{A}\right)^{1/2}\frac{B}{2A}e^{\omega t}\right\} = J_0 - J_1 e^{\omega t} \quad (5)$$

with the ac current out of phase with the ac field.

The current ratio is

$$\frac{J_1}{J_0} = \frac{\sqrt{\Delta E/A}\,B/2A}{1-\Delta E/A} \cong \frac{B}{2A} \cong \frac{\xi_1}{2\xi_0}. \quad (6)$$

The following experimental data are obtained from Fig. 5:

$V_1 = 3\omega\xi_1 = 600$ V/cm,

$V_0 = 13\omega\xi_0 = 2600$ V/cm,

with the dc current $I_0 = 0.18$ A, $J_0 = 6\times10^4$ A/cm^2. Assuming $v_{sat} = 10^7$ cm/s and $\sqrt{\Delta E/A} \cong 1$, the value of n is calculated to be 3.8×10^{16} cm^{-3} for the heated electron density. The value of area A of the GaAs layers is taken to be 3×10^{-3} cm^2. The cold electron density from Hall measurements is 2.98×10^{17} cm^{-3}.

The ac current amplitude I_1 determined from Eq. (6) is 0.021 A, with the ac power generated being 32 mW.

In conclusion, these experiments, while preliminary in nature, demonstrate a new oscillator type which can be readily frequency tuned and whose frequency is not related to the transit time between ohmic contacts. The frequency limitation would appear to be associated with transverse dimensions of the structure. Hess[1] estimates the diffusion time t_r from the expression

$$t_r \cong 4L^2/\lambda_{sat}v_{sat}D, \quad (7)$$

to be $< 10^{-11}$ s for $L_1 = L_2 = 400$ Å, the thickness of the $Al_xGa_{1-x}As$ and GaAs layers, $\lambda_{sat} \sim 10^{-4}$ cm as the mean free path, and $D = 10$ cm^2/s for $Al_xGa_{1-x}As$.

This indicates the oscillator can be extended high into the GHz frequency range. This has not yet been attempted.

The oscillator does not violate Schockley's theorem[14] which states that a homogeneous semiconductor with a negative differential mobility and a well-behaved cathode contact, has a positive differential conductance. In this device, electrons are taken out of one semiconductor GaAs and transferred to a second semiconductor $Al_xGa_{1-x}As$ and do not accumulate or presumably form domains.

The authors would like to thank N. Holonyak, Jr. for his spirited discussions of heterojunctions. He has suggested that this real-space transfer oscillator be called a Hess oscillator in view of Professor Hess' original study of the real-space transfer process. One of the authors (P. Coleman) would particularly like to acknowledge his gifts of vintage tunnel diodes for practice with oscillator circuits. The oscillator work in the Electro-Physics Lab has been sponsored by the Night Vision Laboratory, Ft. Belvoir, VA, under contract DAAK 70-80-C-0066 with R. Buser, R. Shurts, and W. Clark. Work on NDR heterostructures in the Coordinated Science Laboratory has been supported primarily by ONR, Contract N00014-76-C-0806 and ARO Contract DAAG 1980-C-0011. Crystal growth facilities are supported by AFOSR Contract 80-0084 and JSEP Contract N00014-79-C-0429.

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APPENDIX D.

A real space transfer electron device oscillator - a new candidate for the near millimeter range

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Abstract

This paper reports on the demonstration of a new solid state oscillator principle based upon the real space transfer (RST) of electrons from a high mobility GaAs layer to a low mobility AlGaAs layer in a GaAs/AlGaAs heterostructure. The RST of electrons is achieved by applying a DC bias plus the AC field parallel to the layered interface of the heterostructure to periodically heat and cool the electrons. When the electric field increases, the current decreases and a negative differential resistance effect is realized.

The transit time in the oscillator is associated with electron motion across the thin (100-1000 Å) heterostructure layers and not with the electron motion between voltage contacts. A theory of the oscillator predicts it should be capable of generating frequencies well beyond 100 GHz. The power output of the oscillator depends on the number of pairs of GaAs/AlGaAs layers. Since the number of pairs can be made quite large without increasing capacity effects, the total power promises to be substantial.

The RSTED oscillator principle

The RSTED oscillator is based upon a real space transfer[1] of electrons between a high mobility GaAs layer and a low mobility AlGaAs layer in a heterostructure schematically shown in Figure 1.

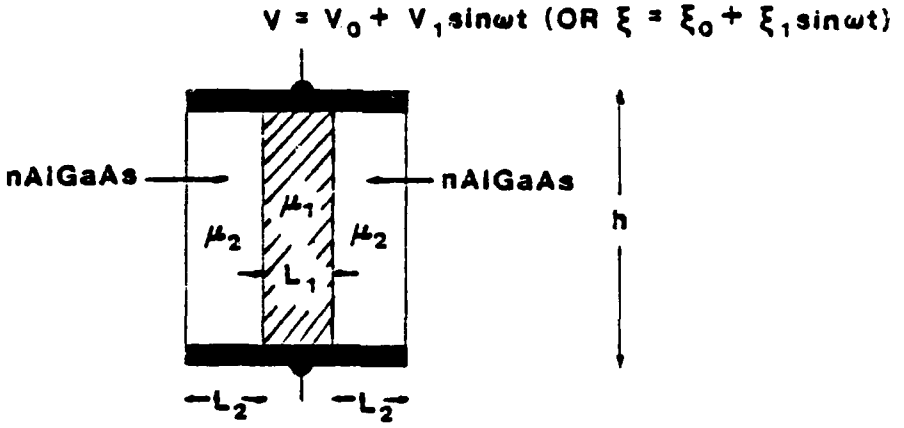

Figure 1. A three-layer GaAs/AlGaAs heterostructure.

A DC bias plus AC oscillating voltage is applied parallel to the layer interfaces to provide the input power to the oscillator and periodically heat the electrons. The resulting current I will have the form

$$I = qAn_1\mu_1\xi - 2qAn_2\mu_2\xi \qquad (1)$$

where $\xi = V/h$ is the electric field, A the area, n the carrier density, q the electric charge, μ_1 and μ_2 the mobilities, and h the height.

Charge conservation in the layers requires that

$$L_1n_1 + 2L_2n_2 = 2L_2N_d^+ \qquad (2)$$

where N_d^- is the doping density in the AlGaAs.

If one constructs a band diagram for the heterostructure[2] and matches the Fermi levels for thermodynamic equilibrium one obtains the condition

$$n_1 e^{-qV_1/kT} = n_2 e^{-qV_2/kT} \tag{3}$$

where qV_1 and qV_2 are the respective barrier energies.

For $kT \ll qV_1$ it is seen that $n_1 \ll n_2$. As kT increases n_1 gets smaller and n_2 gets larger, i.e., a real space transfer occurs where the electrons move back to their original donors in the AlGaAs layers.

If we assume the DC electric field E_0 is sufficiently large to achieve velocity saturation, then the current I can be approximated by the expression

$$I = qAv_s n_1 \tag{4}$$

If we assume $n_1 = (n_{10} - ad)$, then

$$I = qAv_s(n_{10} - ad) \tag{5}$$

where v_s is the saturation velocity and a a constant.

Hence

$$\frac{dI}{dE} = -aqAv_s \tag{6}$$

and we have a negative differential resistance with the current and electric field 180° out of phase, the condition needed for an oscillator.

This RSTED oscillator is a conduction current device with the usual transit time limitation[3] on frequency of operation. However, in this device the transit time is associated with the transverse dimensions of the structure, i.e., the layer thickness. Since the GaAs layer can readily be made 100-400 Å by MBE techniques, this transverse transit time can be made at least a factor of 10 smaller than in a Gunn or IMPATT device.[4]

For example, if one assumes a thermal velocity for the electrons of 2×10^7 cm/sec and a layer thickness L_1 of 200 Å, then the transit time across this layer is seen to be

$$t = \frac{L_1}{v} = \frac{2\times10^{-6}}{2\times10^7} = 10^{-13} \text{ seconds} \tag{7}$$

The minimum RSTED structure is one pair of GaAs/AlGaAs layers which can yield P watts of power. If one increases the structure to N pairs of levels, the power will increase to $P_T = NP$. Thus there is no problem in paralleling oscillators to increase the power output.

Proof of RSTED principle in RF range

The "three period" GaAs/$Al_xGa_{1-x}As$ heterostructure used to demonstrate the RSTED principle is shown in Figure 2.

The heterostructure layers are grown on a high resistance GaAs:Cr substrate using MBE. An undoped AlGaAs buffer layer has been added to further enhance the mobility in the GaAs layer but this may not be necessary for oscillator applications.

The parameters of this structure have not been optimized. Layer thicknesses L_1 and L_2 have been chosen smaller than the depletion and accumulation regions in the AlGaAs and GaAs. The mole fraction x in the $Al_xGa_{1-x}As$ have been chosen to be $x_1 = 0.2$ to yield a barrier height[2] qV_1 of 0.2 eV with the doping density N_d^- of $3\times10^{17}/cm^3$.

Two Au:Ge contacts 1 mm long with a 50 μm spacing were evaporated on the heterostructure surface and then diffused into the three pairs of layers for the ohmic contacts. After

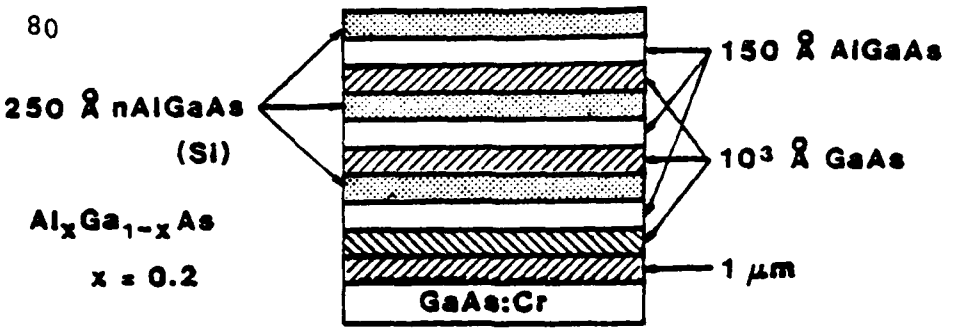

Figure 2. Three-period GaAs/AlGaAs heterostructure.

dicing, the diodes were mounted on a TO-5 header (cap on), wire bonded, and placed in a tunnel diode circuit shown in Figure 3 for tests.

The inductances-capacitances and TO-5 header mounting will limit the frequencies to the RF range but it will be convenient for measurement of the voltages and currents, demonstration of oscillator principle and correlation with theory.

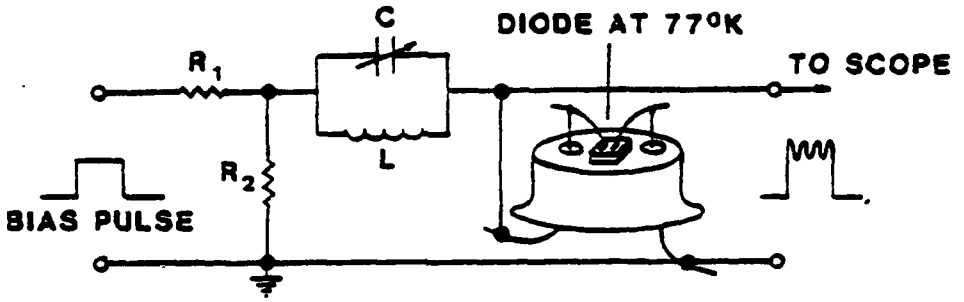

Figure 3. RSTED oscillator RF test circuit.

The I-E curve of the RSTED diode, shown in Figure 4, did not display much if any negative difference resistance. It is expected that the current would saturate at high electric fields due to the variation of the mobility with electric field

$$\mu = \frac{\mu_0}{1 + \frac{q\mu_0 E^2}{\kappa}} \qquad (8)$$

where μ_0 is the low field value and κ a constant. A proof positive of NDR is obtaining oscillation. Current saturation would not yield this effect.

The oscillation behavior of the diode is displayed in Figure 5. It is seen that oscillation is not obtained until the bias pulse exceeds 10 volts as expected from Figure 4. Increasing the bias pulse from 13-20 volts did not appreciable change the RF voltage amplitude.

The oscillation frequency could readily be tuned from 2-25 MHz by changing the value of the condenser indicating that transit time between voltage contacts was not important. The measured parameters of the diode were E_0 = 2600 V/cm, E_1 = 600 V/cm, I_0 = 200 mA, and I_1 = 15 mA, to yield an RF power of 23 mW, i.e., about 8 mW per pair of layers or $3 \cdot 10^3$ watts/cm^3 of GaAs.

Thermionic emission model for RSTED oscillator

It will be assumed that the DC bias field E_0 is sufficiently large to saturate the electric velocity v_s in the GaAs layer and that the energy transfer between layers is small.

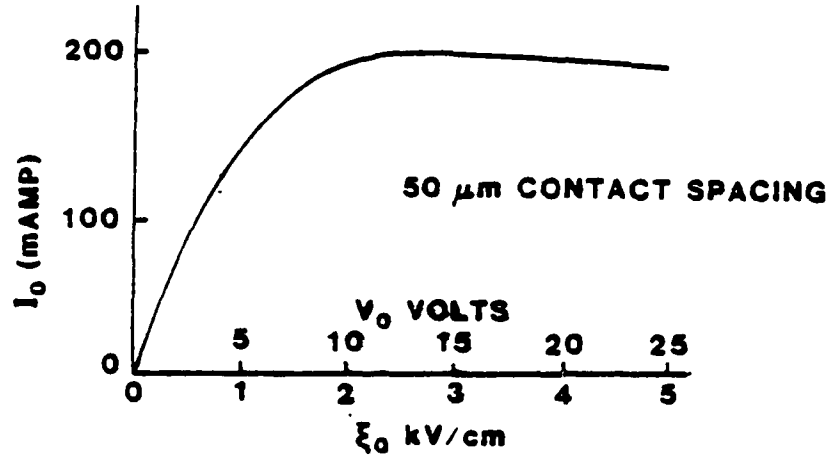

Figure 4. I-V (or I-ξ) characteristics of diode 337 at 77°K.

The power balance equation can then be approximated as

$$q L_1 n_1 v_s \xi = \frac{3k(T_1-T_0)}{2\tau} L_1 n_1 + L_1 n_1 \frac{d}{dt} \frac{3k(T_1-T_0)}{2} \tag{9}$$

or

$$q v_s \xi = \frac{3k(T_1-T_0)}{2\tau} + \frac{d}{dt} \frac{3k(T_1-T_0)}{2} \tag{10}$$

where the term on the left is the power input, the first term on the right the power going into the crystal lattice at temperature T_0 and the last term the change in heat capacity of the electron gas. The τ quantity is the energy relaxation time.

The particle flow balance is given by the equation

$$2 n_1 v_1 e^{-qV_1/kT_1} - n_2 v_2 = - L_1 \frac{dn_1}{dt} = 2L_2 \frac{dn_2}{dt} \tag{11}$$

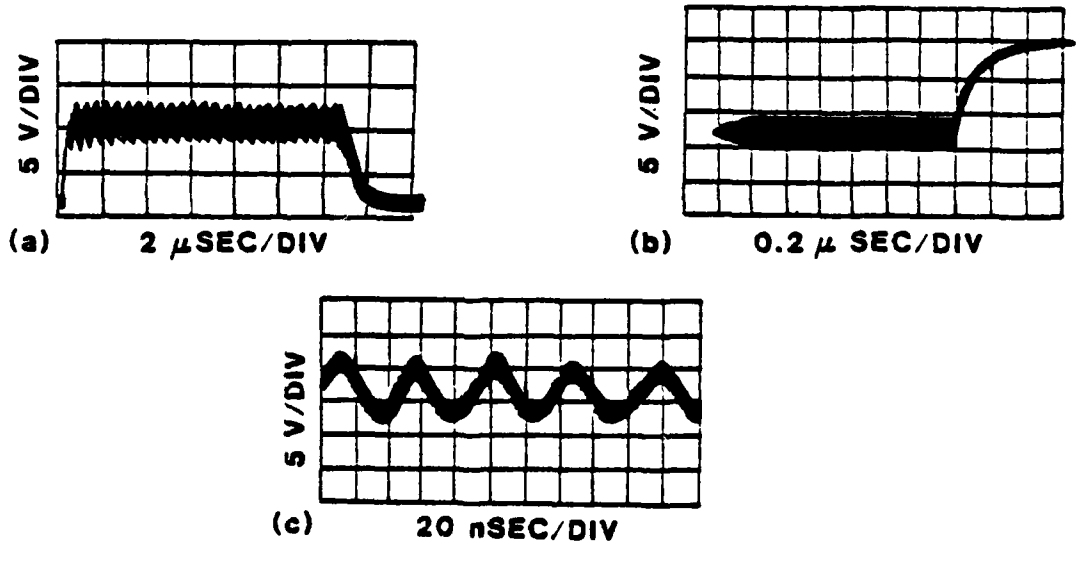

Figure 5. Oscillation behavior of a NDR GaAs/nAlGaAs heterostructure. a) at 2 MHz, b) at 25 MHz, c) at 25 MHz expanded.

where $v_1 = \sqrt{\frac{kT_1}{2\pi m^*}}$ and $v_2 = \sqrt{\frac{kT_2}{2\pi m^*}}$ and it has been assumed that the barrier height qV_2 is negligible.

The temperature T_2 of the AlGaAs layer is assumed to remain fairly constant, hence the problem reduces to three unknowns, T_1, n_1, and n_2 and three equations, (2), (10), and (11).

Assume a Fourier expansion of the following terms

$$\mathcal{E} = \mathcal{E}_0 + \mathcal{E}_1 \sin\omega t \tag{12a}$$

$$kT_1 = (kT_0 + x_{01}) + x_1 \sin\omega t = x_0 + x_1 \sin\omega t \tag{12b}$$

$$n_1 = N_{10} + N_1 \cos\omega t - M_1 \sin\omega t \tag{12c}$$

$$n_2 = N_{20} + N_2 \cos\omega t + M_2 \sin\omega t \tag{12d}$$

$$I = I_0 + I_1 \sin\omega t + I_2 \cos\omega t \tag{12e}$$

with

$$e^{-qV_1/kT_1} = e^{-\frac{qV_1}{x_0 + x_1 \sin\omega t}} = e^{-\frac{qV_1}{x_0}} e^{\frac{qV_1 x_1}{x_0^2 \sin\omega t}} = e^{-\frac{qV_1}{x_0}} + b_1 \sin\omega t \tag{12f}$$

The following results are obtained

$$x_0 = kT_0 + \frac{2q\tau v_s \mathcal{E}_0}{3} \tag{13}$$

$$x_1 = \frac{2q\tau v_s \mathcal{E}_1}{2[1 + (\omega\tau)^2]} = \frac{2q\tau v_s \mathcal{E}_1}{3} \tag{14}$$

$$b_1 = \frac{qV_1}{x_0^2} x_1 e^{-qV_1/x_0} \tag{15}$$

and

$$-\frac{I_1}{I_0} = \frac{M_1}{N_{10}} = \frac{2b_1 \, 2e^{-qV_1/x_0} + \frac{v_2 L_1}{v_1 L_2}}{\left(\frac{\omega L_1}{v_1}\right)^2 + \left(2e^{-qV_1/x_0} + \frac{v_2 L_1}{v_1 L_2}\right)^2} \tag{16}$$

The transit time is seen in Equation (16) in the $\frac{\omega L_1}{v_1}$ term whose magnitude is desired to be small, i.e.,

$$\frac{\omega L_1}{v_1} < 1 \quad \text{or} \quad \frac{1}{2\pi f} > \frac{L_1}{v_1} \tag{17}$$

The value of $v_2 L_1 / v_1 L_2$ for the structure was the order of one although it would be desirable to have this term smaller. Hence the expression for the current ratio is for a single pair of layers

$$\frac{I_1}{I_0} = -2 \frac{qV_1}{x_0} \frac{x_1}{x_0} e^{-\frac{qV_1}{x_0}} \tag{18}$$

Assuming $\tau v_s = 4 \times 10^{-5}$ cm, $\mathcal{E}_0 = 2600$ V/cm, $\mathcal{E}_1 = 600$ V/cm and $T_0 = 77°K$, the value of I_1/I_0 for three pairs of layers is calculated to be -0.072 compared to the experimental ratio 15/200 = -0.075.

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